

# Monolithic CMOS Pixel R&D for the ILC at LBNL

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# CMOS Pixel Sensors LDRD at LBNL



CMOS Monolithic Pixel program for the ILC approved under the Laboratory-directed R&D (LDRD) program for 3 years (FY05-07)

Project funding covers setting up a dedicated Si pixel detector test facility, IC designers, foundry submissions, salaries for one postdoc one GSR and visitors

**Pursue R&D to optimise pixel geometry, achieve improved charge collection capability, noise suppression, fast read-out and data sparsification:**

**Implement active reset functionality:**

- reduce kTC noise
- reduce fixed pattern noise

**Evaluate OPTO process:**

- thicker epi-layer
- reduced leakage current

Define sensor specs based on full simulation of benchmark reactions including machine induced backgrounds and material effects;

Develop engineered design of Vertex Tracker based on CMOS sensors.

# Pixel Detector R&D at LBNL



Hybrid Pixel Detector for ATLAS (K. Einsweiler, Physics)

CMOS Pixel R&D for STAR Vertex Upgrade (H. Wieman, Nuclear Science)

CMOS Pixel R&D for Electron Microscopy (P. Denes, Engineering)

CPCCD for experiments at Synchrotron Light sources (P. Denes, Engineering)

Thick CCD sensors for SNAP/JDEM (SNAP Group, Physics)

ILC LDRD aims at addressing key R&D issues exploiting synergies and opportunities at the interface between different fields and applications.

# Si Pixel Detector Test Facility



Pixel test facility using collimated  $^{55}\text{Fe}$  X Ray and Laser Beams

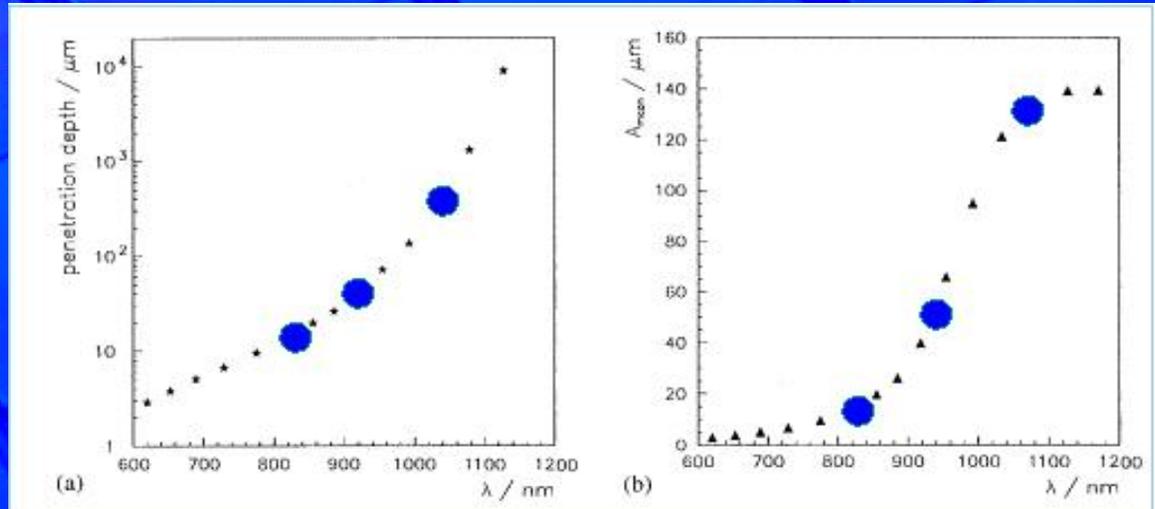
Setting up laser system to mimic m.i.p. in Si:

Diode lasers driven by fast pulse generator to produce laser pulses from 0.5 - 100 ns

laser beam collimated to  $< 5 \mu\text{m}$

choice of laser wavelengths to probe charge collection through detector thickness

synchronise with DAQ and computer controlled high-accuracy XY stages to perform automated scans



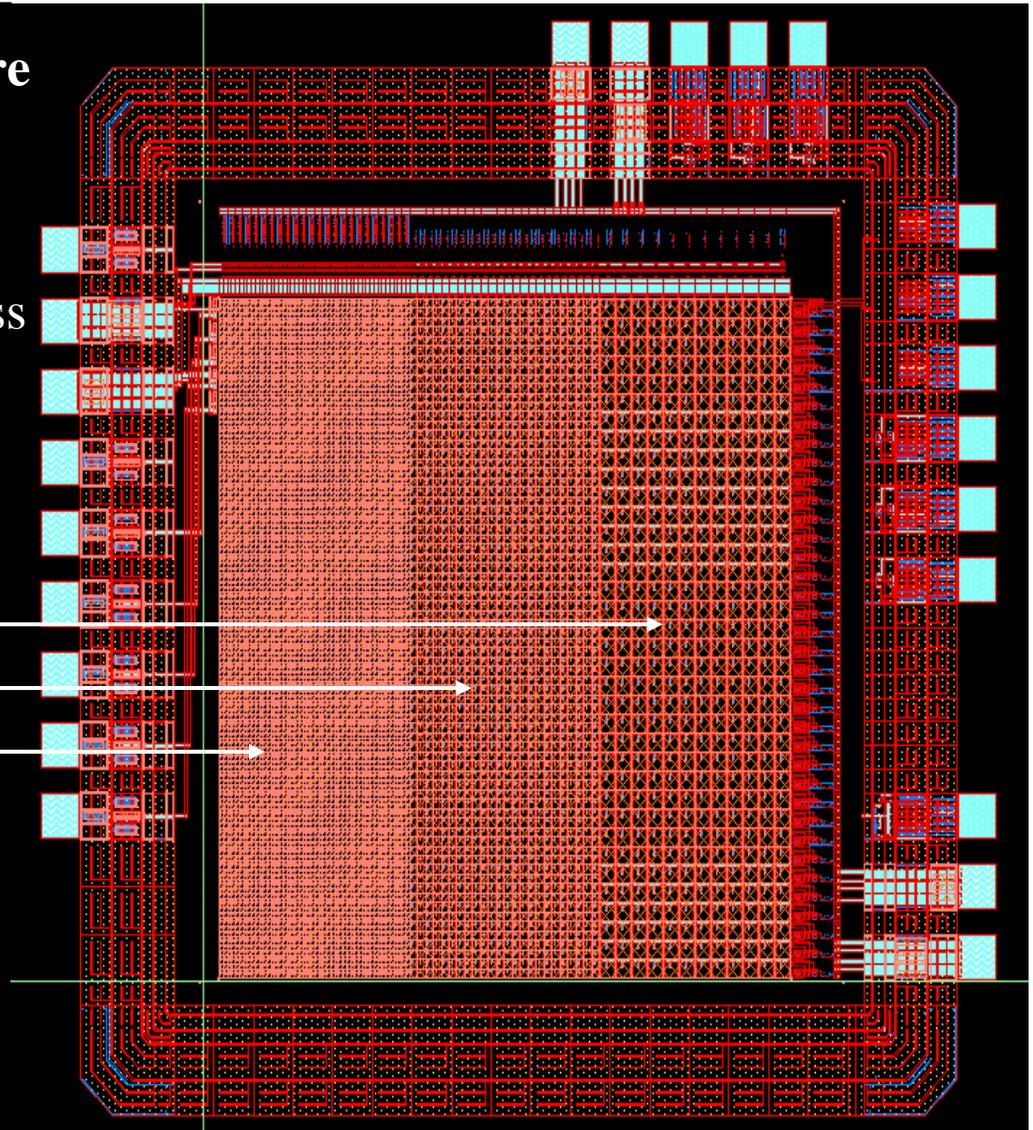
# 0.25 OPTO AMS Test Structure



## Development of LDRD Test Structure

- design in collaboration with LBNL Engineering Division (P. Denes):
- Submission in April 05
- AMS 0.35 $\mu\text{m}$  CMOS-OPTO process through MOSIS:  
14 $\mu\text{m}$  epi layer, low dark current
- **Three Pixel Geometries**
  - 12 x 36 40  $\mu\text{m}$  pixels
  - 24 x 72 20  $\mu\text{m}$  pixels
  - 48 x 144 10  $\mu\text{m}$  pixels

Expect test structures back from foundry in June to be tested during Summer, second generation in FY06



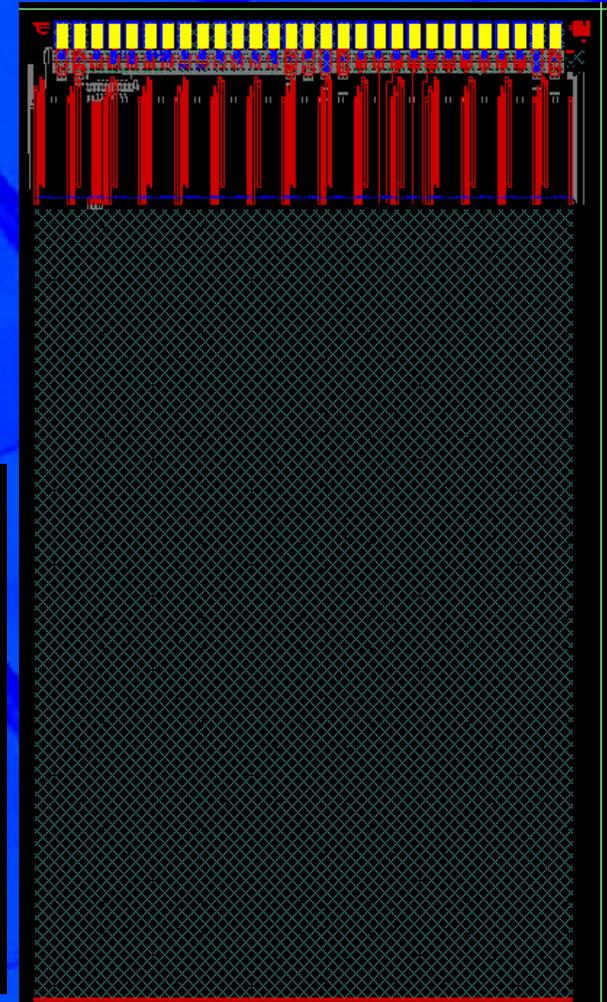
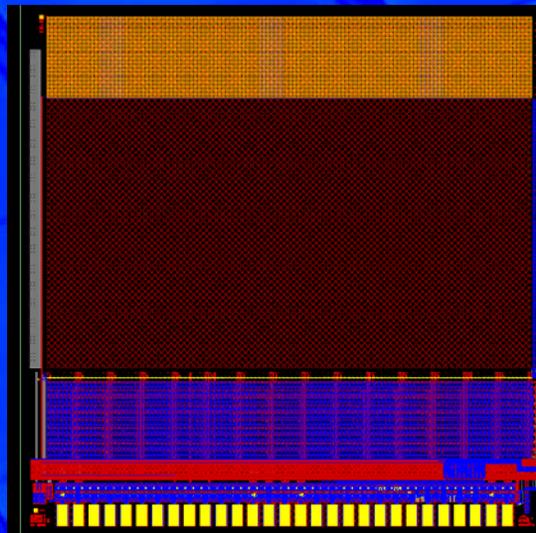
# 0.25 TSMC CDS Test Structure



Two set of structures in TSMC 0.25  $\mu\text{m}$  designed at LBNL (P. Denes) and tailored to electron microscopy applications

- 6x6  $\mu\text{m}$  and 19x19  $\mu\text{m}$  pixels
- on-pixel capacitor for CDS
- per-column 10 bit ADC
- radiation tolerant layout

submitted February 05  
characterisation with  
 $^{55}\text{Fe}$  source and pulsed laser  
in Summer 05



# 0.50-AMIS Test Structure

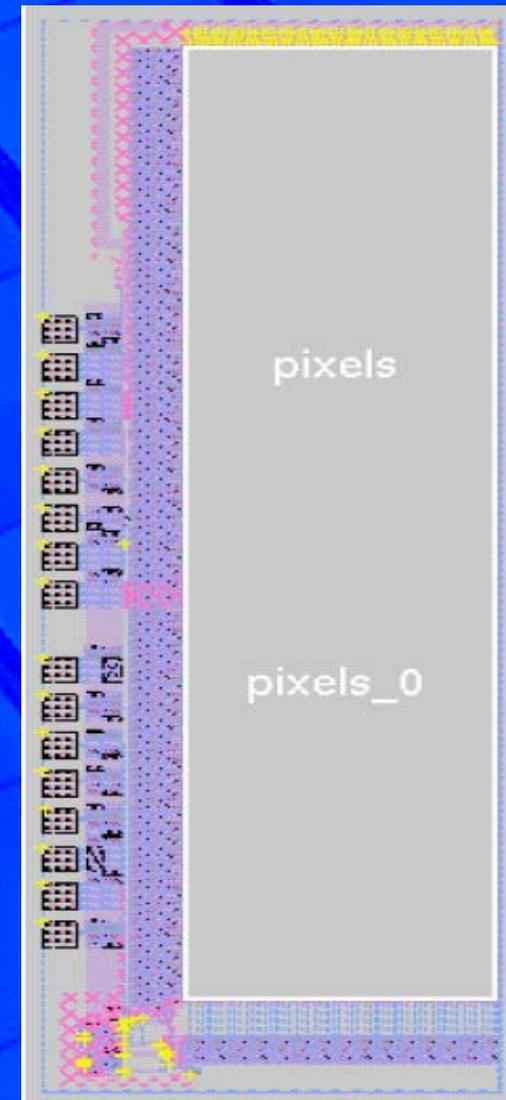


Pixel structure designed at UC Irvine (S. Kleinfelder) in collaboration with LBNL STAR group

- 3T pixels 20 mm pitch and 13  $\mu\text{m}$ , 20  $\mu\text{m}$ , 32  $\mu\text{m}$ , 41  $\mu\text{m}$ , 54  $\mu\text{m}$  diode size
- 0.50  $\mu\text{m}$  AMIS C5 process

submitted in October 04 and presently under test

Additional Test Structure with 5, 20 and 30  $\mu\text{m}$  pixels

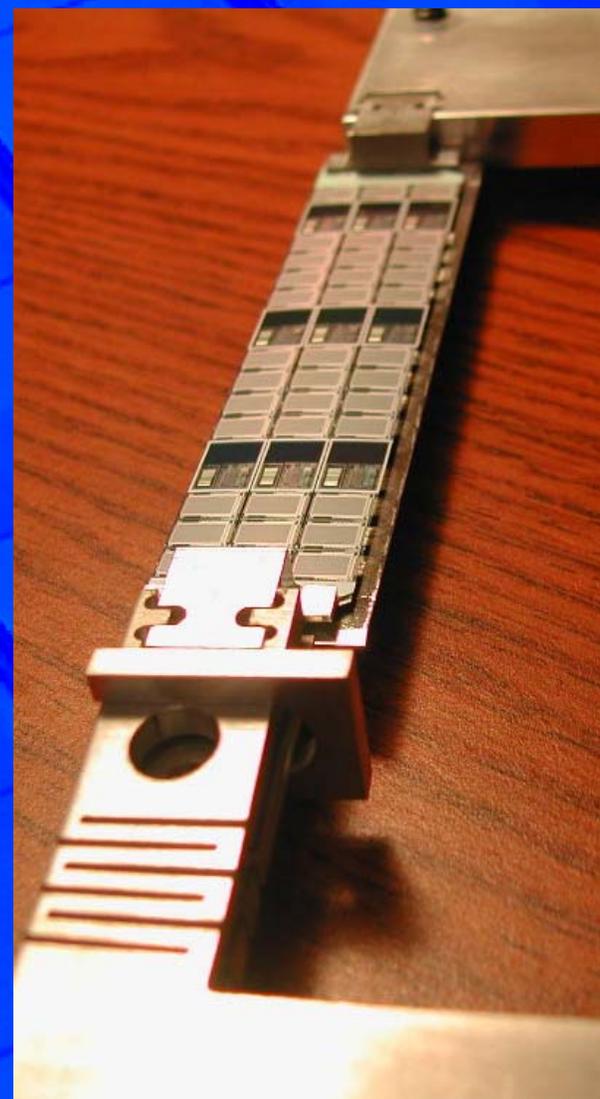


# Sensor Backthinning



First tests of MIMOSA chip backthinning by LBNL STAR group successful to  $50\mu\text{m}$

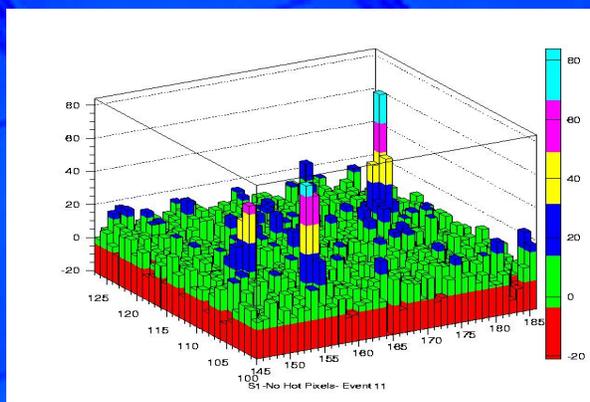
Plan to perform repeated essays of sensor backthinning from US vendors and functionality tests



# $^{55}\text{Fe}$ Test of Backthinned MIMOSA V Chips

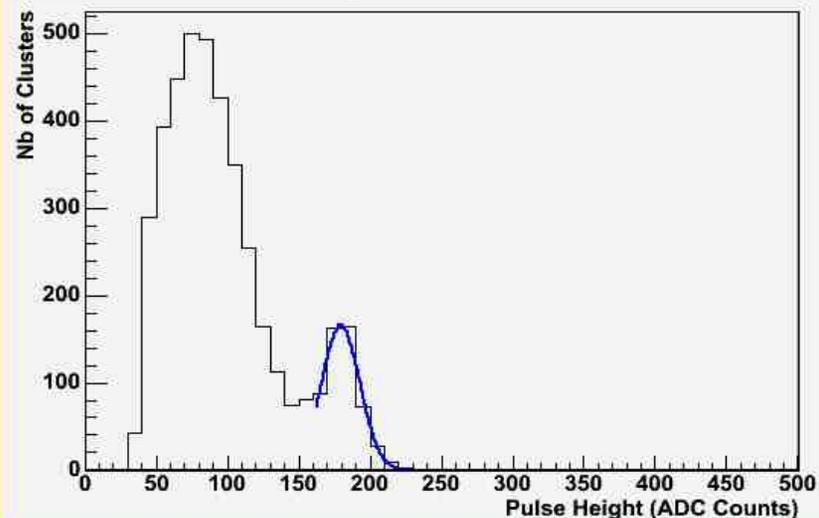


Test performed with  $^{55}\text{Fe}$  source:  
read 2 subsequent frames of 512x128 pixel  
array  $\rightarrow$  Online CDS, pedestal subtraction,  
rms calculation  $\rightarrow$  Offline ROOT-based  
Cluster analysis

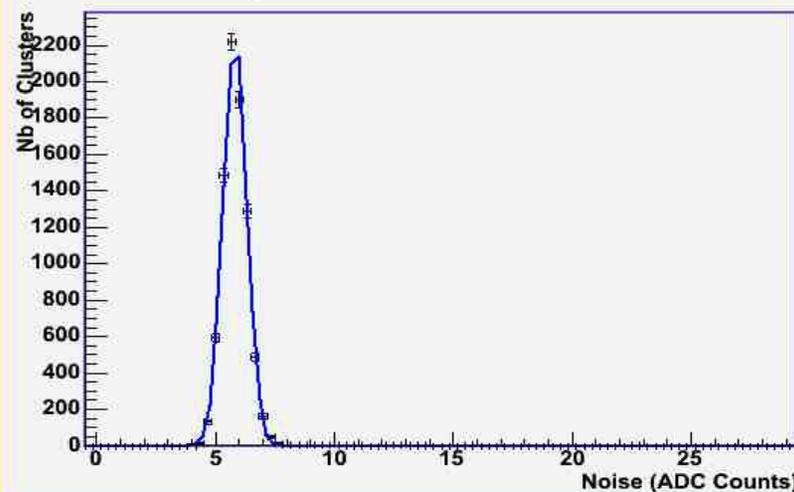


Cluster Multiplicity	1.65
ENC Noise	50.
S/N	15.

Single Pixel Pulse Height



Single Pixel Noise

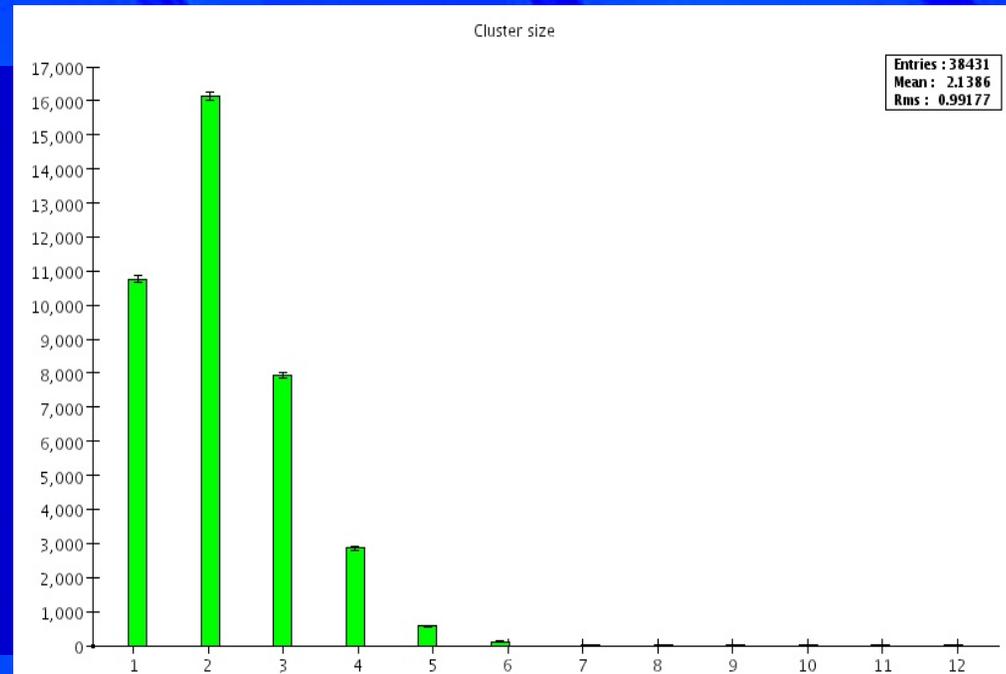
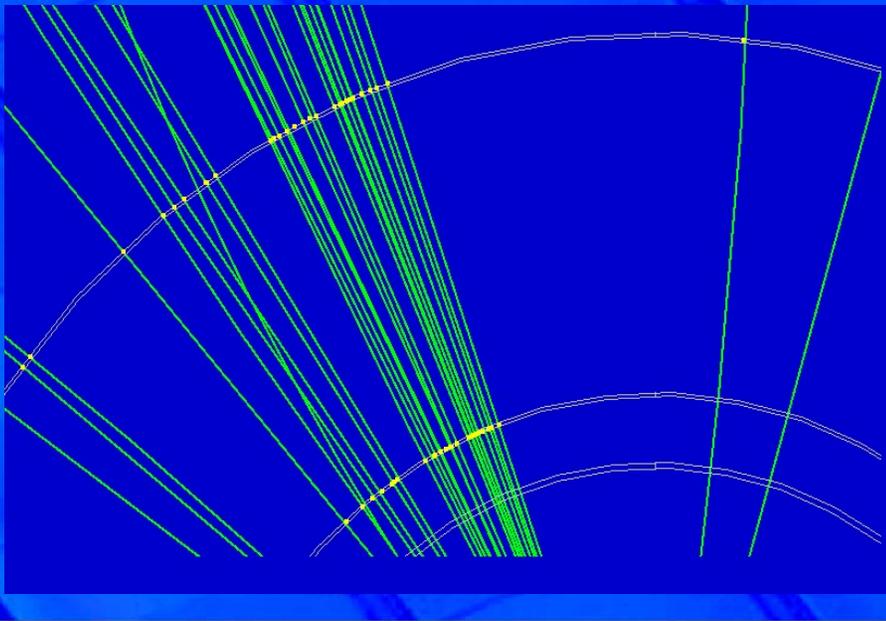


# Simulation studies



Study two-track separation and cluster merging using pixel response from LBNL Lab test and CERN test beam results (MIMOSA V and IX) in collaboration with Strasbourg

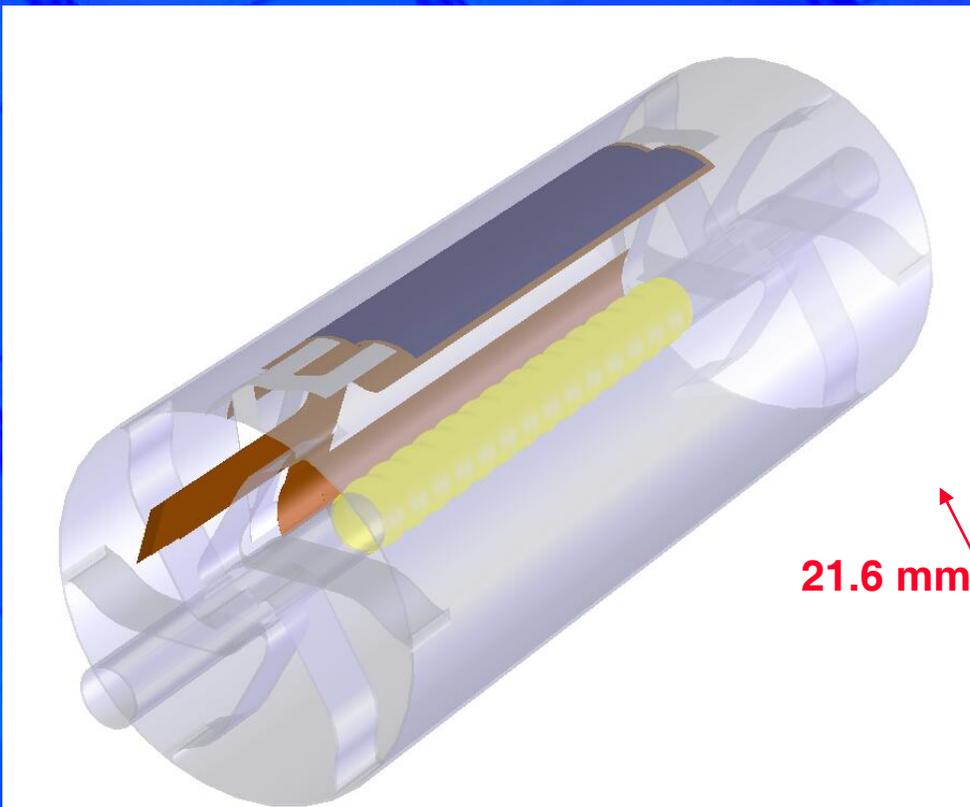
Tune and customize **hep.lcd.CcdSim** digitisation code written in Java by N. Sinev to CMOS pixel response and perform study on selected benchmark processes:



# Vertex Tracker Engineering Design

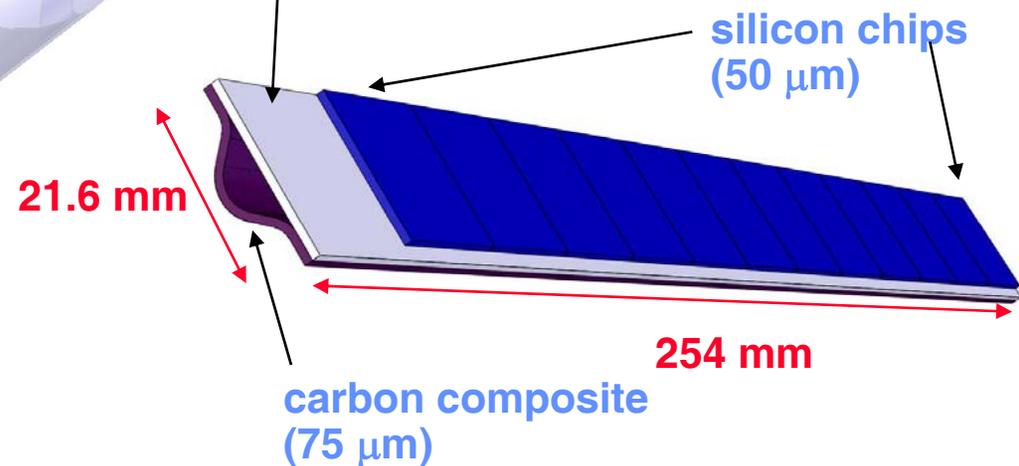


Important experience being accumulated with STAR Vertex Detector to be transferred to engineering design for ILC Vertex Tracker



Construction of first prototype Pixel ladder with back-thinned MIMOSA V chips, driver electronics and carbon composite support:

aluminum kapton cable  
(100  $\mu\text{m}$ )





ILC CMOS Pixel R&D started at LBNL supported by LDRD funding in collaboration with Engineering & Nuclear Science Divisions;

Important synergy with Pixel detector R&D aimed at Biology and Material Science applications and STAR project at RHIC;

Started testing existing CMOS test structures and planned for first submission;

FY05 devoted to sensor geometry optimisation based on Lab data and full detector simulation of benchmark reactions.