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# READ OUT CARD (ROC) DESIGN PROPOSAL

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## INTRODUCTION

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The Read Out Card (ROC) sits in the PHENIX IR next to the FPIX/sensor assembly and is needed to interface the read out chips (FPIX) with the FEM (Front End Module). It needs to provide the following functionalities:

1. Read in serial data from  $N$  FPIX chips via 1, 2 or 4 LVDS pairs (depending upon data throughput needs).
2. Strip off the sync words, process and combine data words from several FPIX into a single 28-bit parallel stream: 24-bit FPIX word + 4-bit Chip ID.
3. Send out the parallel data to SERDES and out to the FEM via fiber.
4. Output BCO clock and Readout clock (LVDS) to FPIX.
5. Output FPIX control signals (LVDS) including firefighter reset (FFR), shift control (SHIFT\_CTRL) and shift in (SHIFT\_IN) signals.
6. Implement slow control interface with FEM to download commands.
7. Calibration pulses based on FEM control.

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## DESIGN REQUIREMENTS

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Based on ROC functionality we find that there are two main drivers for the design:

1. **Radiation Tolerance:** Since the ROC will sit in the PHENIX IR, it will need to be radiation tolerant. Traditional SRAM based FPGAs, like those by Xilinx and Altera can undergo Single Event Upsets (SEU) and lose their configuration, leading to a malfunction. Although both Xilinx and Altera offer “scrubbing” software, which however requires reload of the configuration. This is not acceptable during data taking. Based on a study by Mark Prokop there can be several upsets per hour for Xilinx/Altera chips even for RHIC I Au+Au rates. In comparison, flash based chips made by Actel have negligible SEUs (see Table 1 for details).
2. **LVDS IOs:** Since all I/O to FPIX is LVDS, we need to maximize the number of LVDS pairs per FPGA. Actel allows most I/O pins to be used as LVDS, e.g. Actel A3PE600 FPGA permits 65 to 135 LVDS pairs depending upon package.

Based on above two considerations we have decided to go with the Actel ProASIC3/E family (exact FPGA will depend upon throughput requirements and segmentation).

	<b>Actel Axcelerator</b>	<b>Actel ProASIC3</b>	<b>Altera Stratix II GX</b>	<b>Altera Cyclone II</b>
Model	AX 2000	A3PE3000	EP2SGX60	EP2C70
Configuration type	Anti-fuse	FLASH	SRAM	SRAM
Radiation Tolerance	200kRad	200kRad	50kRad	50kRad
Single-ended I/O / Differential I/O pairs	684 / 342	616 / 300	534 / 78	622 / 262
Voltages	1.5	1.5	1.2	1.2
Power (Quiescent)	22mA	25mA	820mA	250mA
Built-in SERDES	No	No	Yes	No
I/O Rates	LVDS - 700 Mb/s	LVDS - 700 Mb/s	LVDS-6.375 Gb/s	LVDS-622 Mb/s
Configuration Errors	No	No	Yes	Yes
SEE types	clocks, data memory	clocks, data memory	configuration, clocks, memory, SERDES	configuration, clocks, memory
SRAM Memory- Data	294912	516096	6747840	1152000
SRAM Memory- Configuration	0	0	16951824	14319216
FLASH Memory- Configuration	0	0	32 Mbyte	16 Mbyte
RHIC I AuAu SEU Rate - 10 cm /hr-chip	0.00	0.00	27.12	22.91
RHIC I AuAu SEU Rate - 40 cm /hr-chip	0.00	0.00	1.70	1.43
RHIC II AuAu SEU Rate - 10 cm /hr-chip	0.00	0.00	271.23	229.11
RHIC II AuAu SEU Rate - 40 cm /hr-chip	0.00	0.00	16.95	14.32
RHIC II p+p SEU Rate - 10 cm /hr-chip	0.00	0.00	2169.83	1832.86
RHIC II p+p SEU Rate - 40 cm /hr-chip	0.00	0.00	135.61	114.55
Total Integrated Dose	>200k	>200k	>50k	>50k

Table 1: Radiation tolerance for different FPGAs.

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## IMPLEMENTATION

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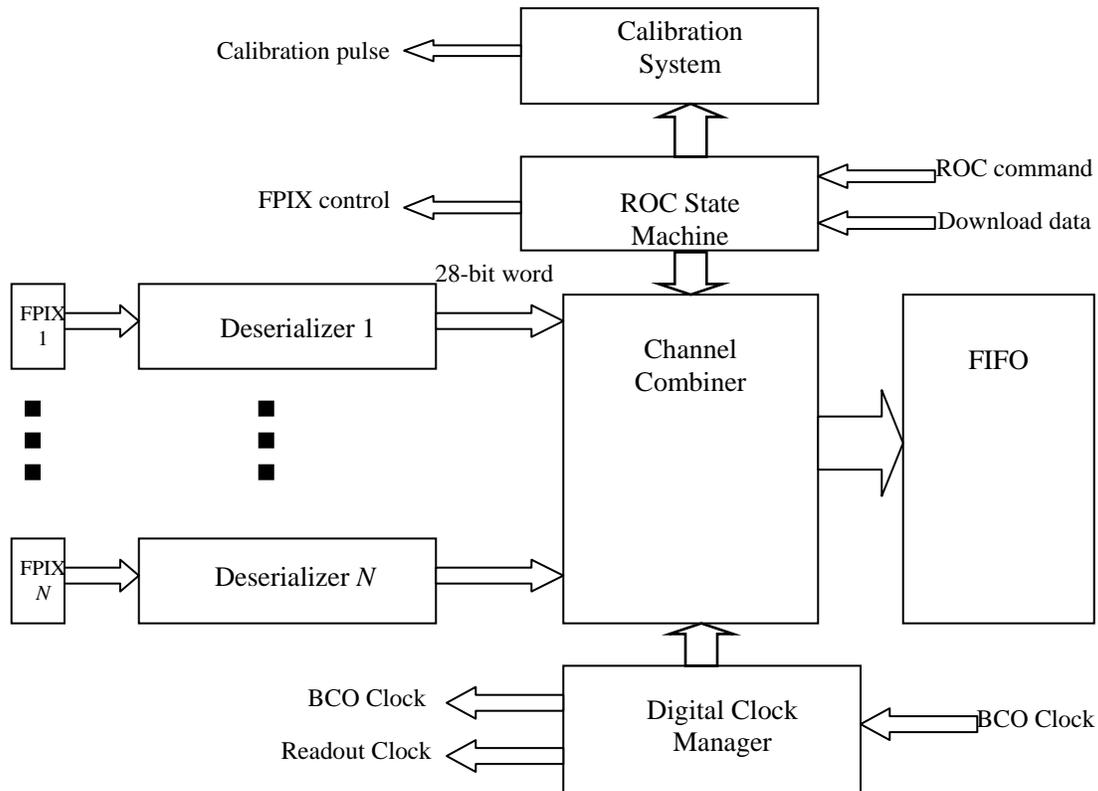


Figure 1: Block diagram for ROC.

- **Deserializer:** Takes LVDS input (1, 2 or 4 lines) from each FPIX and uses shift registers to deserialize the stream into 24-bit parallel words. It is clocked using the internally generated readout clock (MCLK), the same clock that is sent to FPIX. Each deserializer individually checks for synchronization with each FPIX and appends a 4-bit Chip ID to the data word (making it 28-bit).
- **Channel Combiner:** Uses a multiplexer and counter to combine the 28-bit words from  $N$  deserializers into a single stream. It then strips off the sync words and sends the data words into the FIFO.
- **FIFO:** Buffers data words and sends them to SERDES.
- **Digital Clock Manager:** Manages different clock domains. Takes BCO clock input and sends it to FPIX, Also generates the MCLK along with other clocks for FIFO/SERDES operations.
- **Calibration:** Talks to Pat's calibration board and sets pulse height/timing. This calibration board is described in more detail in a later section.

- **ROC State Machine:** Receives commands via slow control (currently via USB) and sends appropriate responses to FPIX (e.g. firefighter reset or download shift in) and other components like calibration, channel combiner etc.

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### FPIX PULSER BOARD

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A pulser board for calibration was designed by Pat McGaughey, using a Texas Instruments 10-bit dual DAC (TLV5617A) along with a resistor capacitor network for pulse shaping. It can be controlled through a parallel port interface.

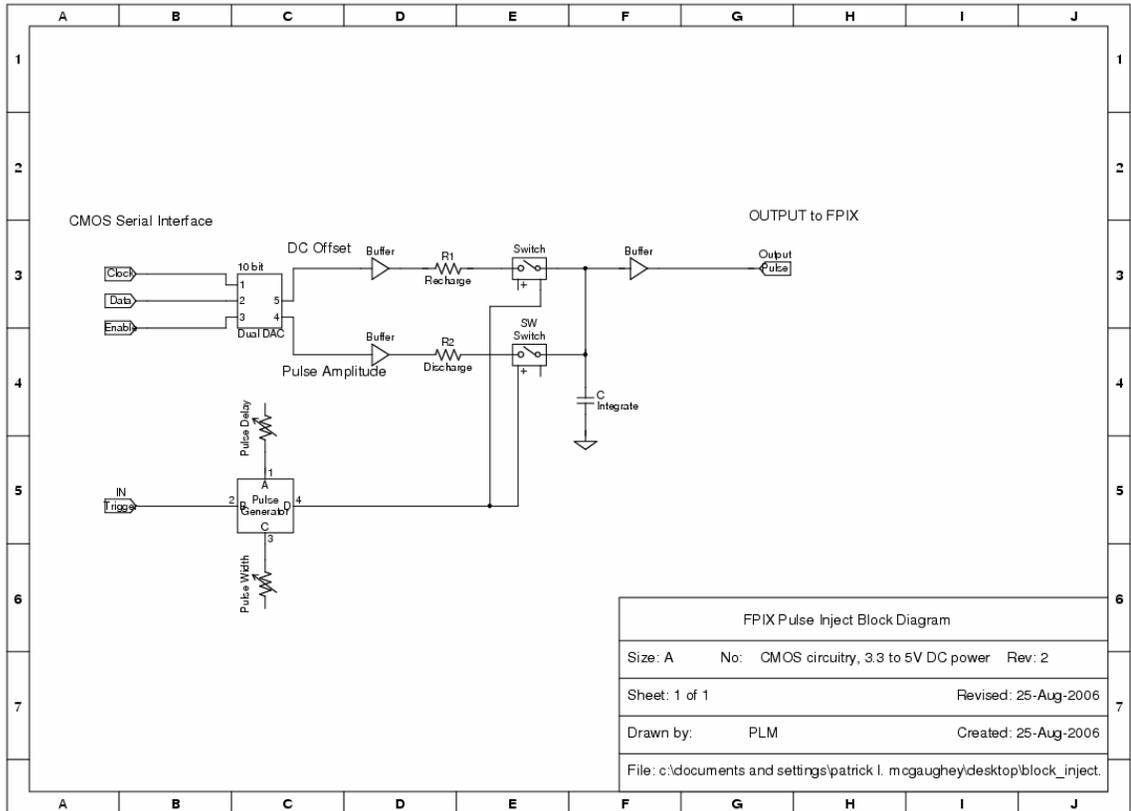


Figure 2: Schematic for FPIX Pulser board (by Pat McGaughey).

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### TIMING AND SEGMENTATION

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Segmentation, i.e., mapping from number of FPIX to ROC to fiber depends primarily upon latency requirements: 424 ns for Lvl-1 and 40  $\mu$ s for PHENIX DAQ. The plot below (by Sergey Butsyk) shows the latency (in BCO clock ticks) vs. # chips/fiber for a central Au+Au event (10 hits per chip) for different numbers of readout lines:

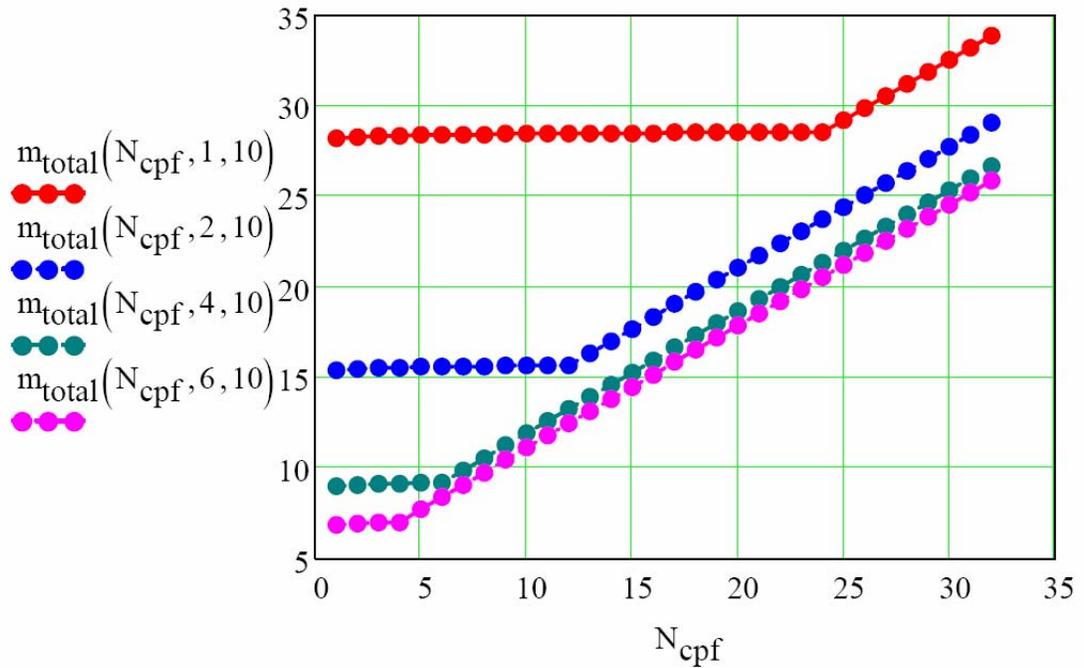


Figure 3: Latency (in BCO ticks) vs. #chips/fiber for different number of readout lines (assuming 10 bits/chip and ~3 Gbps fiber).

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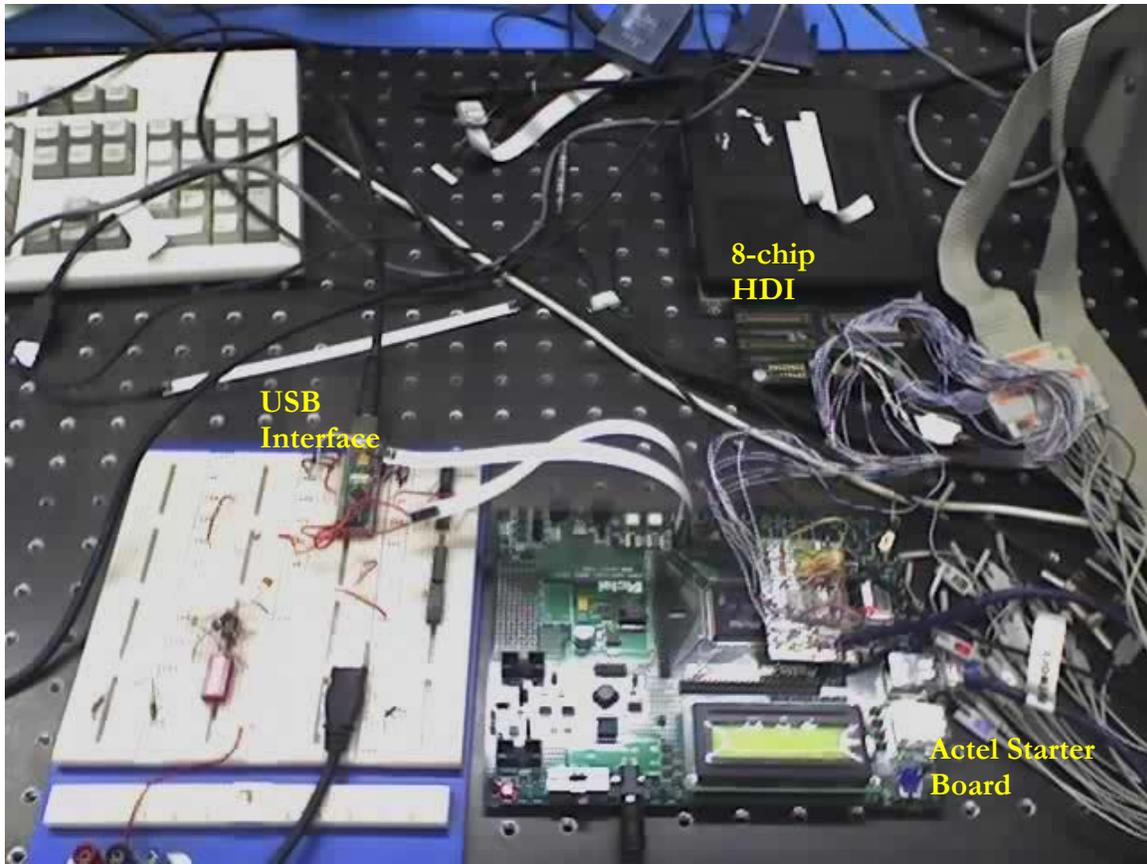
#### CURRENT STATUS

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A prototype design has been implemented on an Actel ProASIC3 A3P250 FPGA (using VHDL) on an Actel starter board. Unfortunately the starter board does not allow setting 2.5 V on all I/O banks leading to a paucity of available LVDS pairs (12 pairs). As a result we can either:

- A) Read out 4 chips with 1 line each.
- B) Read out 1 chip with up to 4 lines readout.

The current prototype as assembled in the lab is shown below:



*Figure 4: Lab setup of the 8-chip module readout, using Actel starter board.*

It has the following features:

1. Reads out 4 chips from an 8-chip module. Here is the output from the logic analyzer showing: MCLK, SYNC\_WORD, VALID, CHIP\_ID as well as lower two bits of DATA, indicating that SEND\_DATA has been enabled for Chip ID = 4.

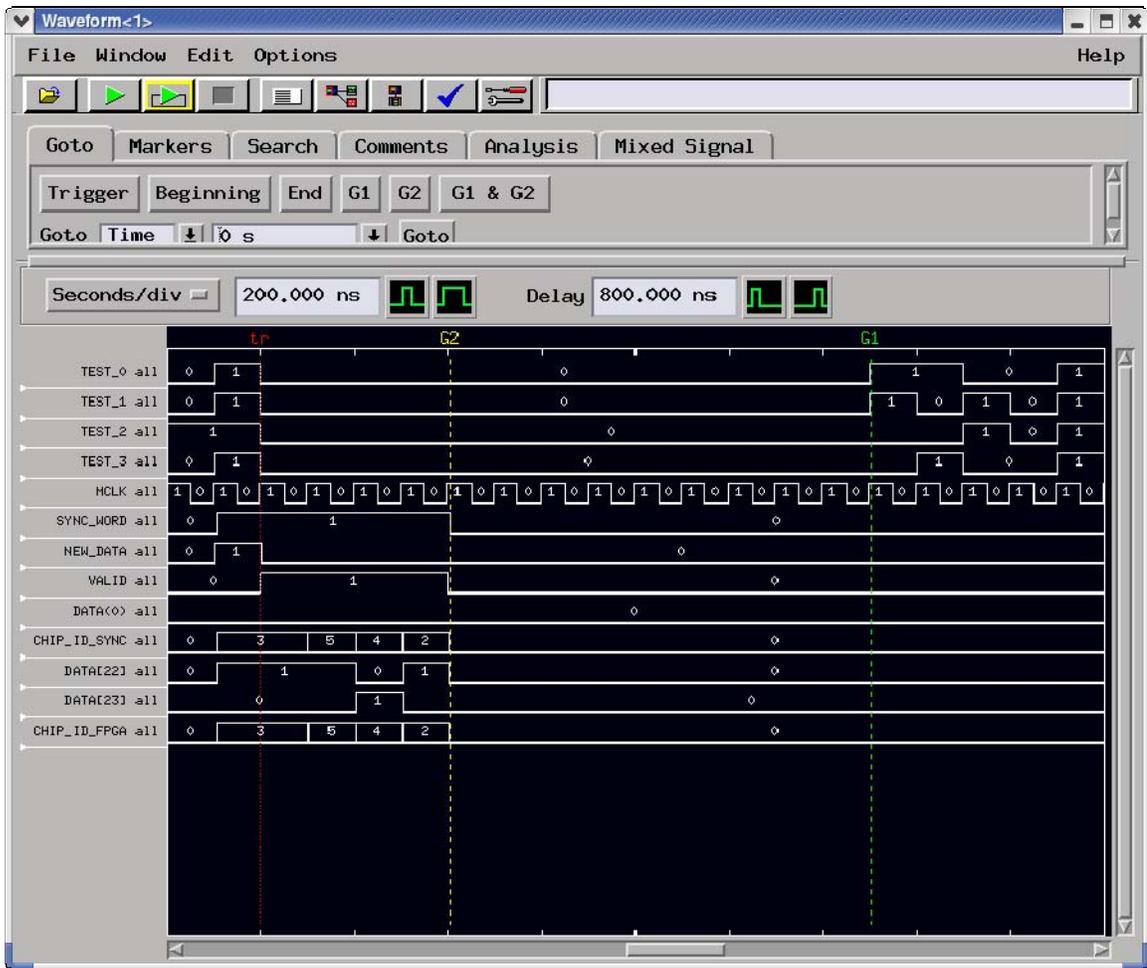


Figure 5: Logic analyzer output showing readout from 8-chip module.

2. Implements slow controls via USB using DLP-2232M-G USB Adapter from [dlpdesign.com](http://dlpdesign.com).
3. A simple Tcl/Tk GUI allows user to either do a firefighter reset or download commands into FPIX.



Figure 6: Simple Tcl/Tk GUI to control FPIX via USB port.

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## TO DO

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In order to do high speed readout continuously we are using National Instruments DigiIO NI 6534 PCI card, which is capable of taking 32-bit data at up to 20 MHz. A prototype PCB is being designed for the Actel A3PE600 with 35 LVDS pairs, which will allow us to readout an 8-chip with at least 2 lines each. It will include a USB interface for slow control as well as the pulser module.