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The Pinned Photodiode

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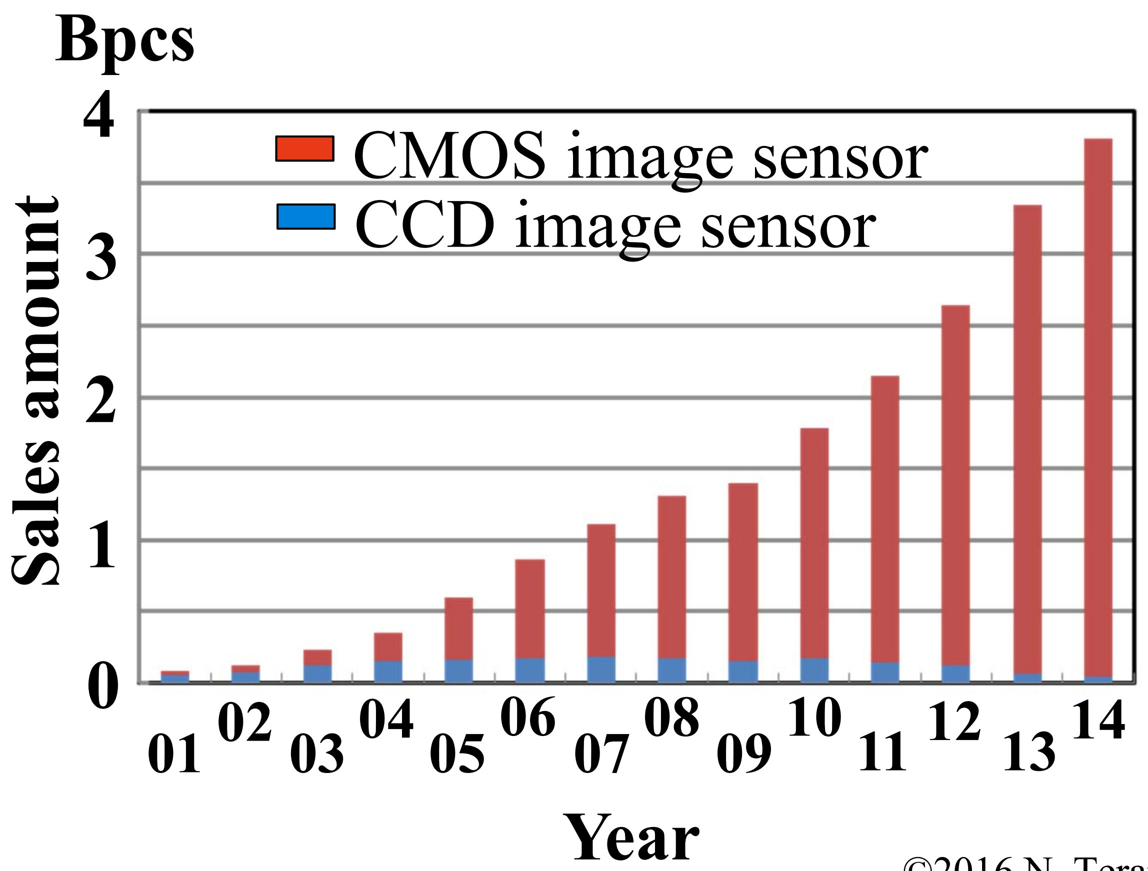
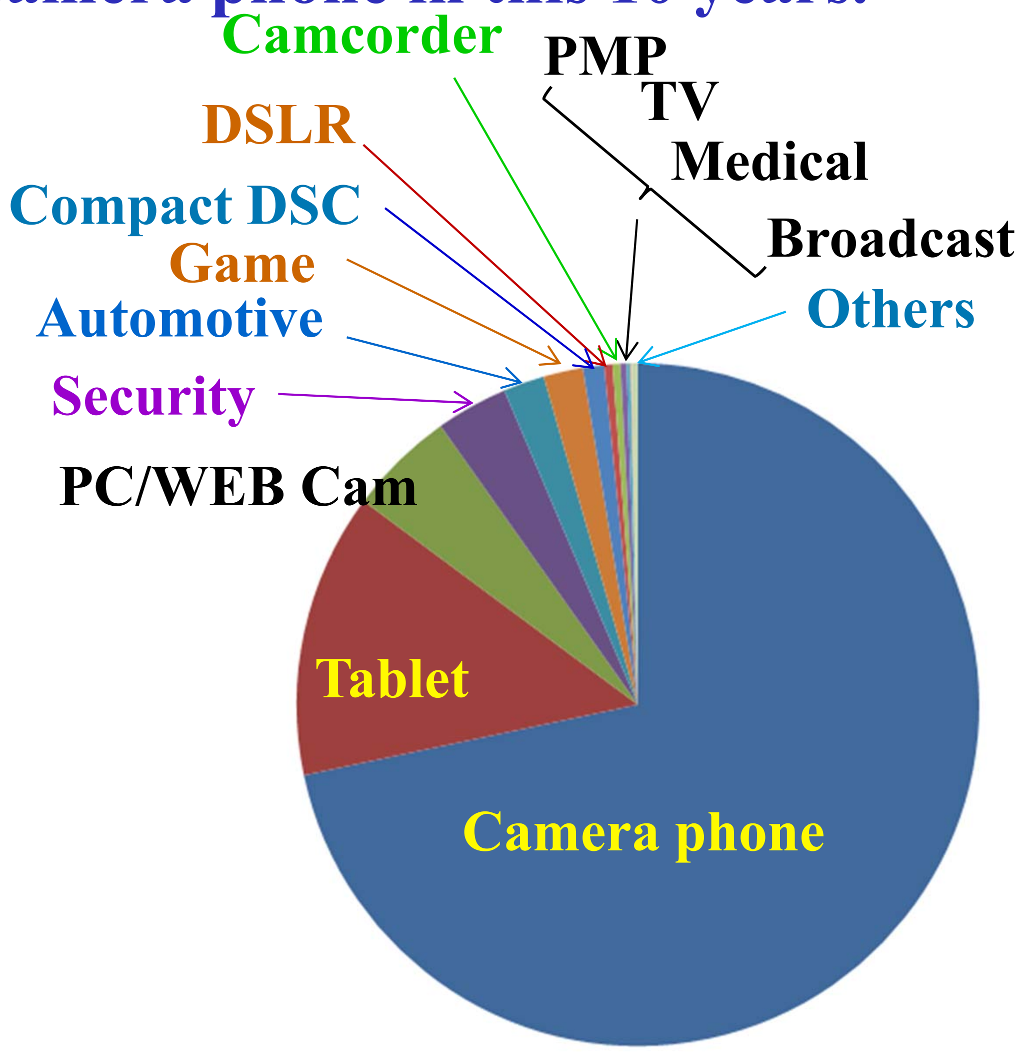
Image Sensor (IS) Market

- IS sales amount has grown mainly by camera phone in this 10 years.
  But, it became diminished in Q4, 2015.
- IS spreads into various applications,
  "Others" includes scientific,
  industrial, …



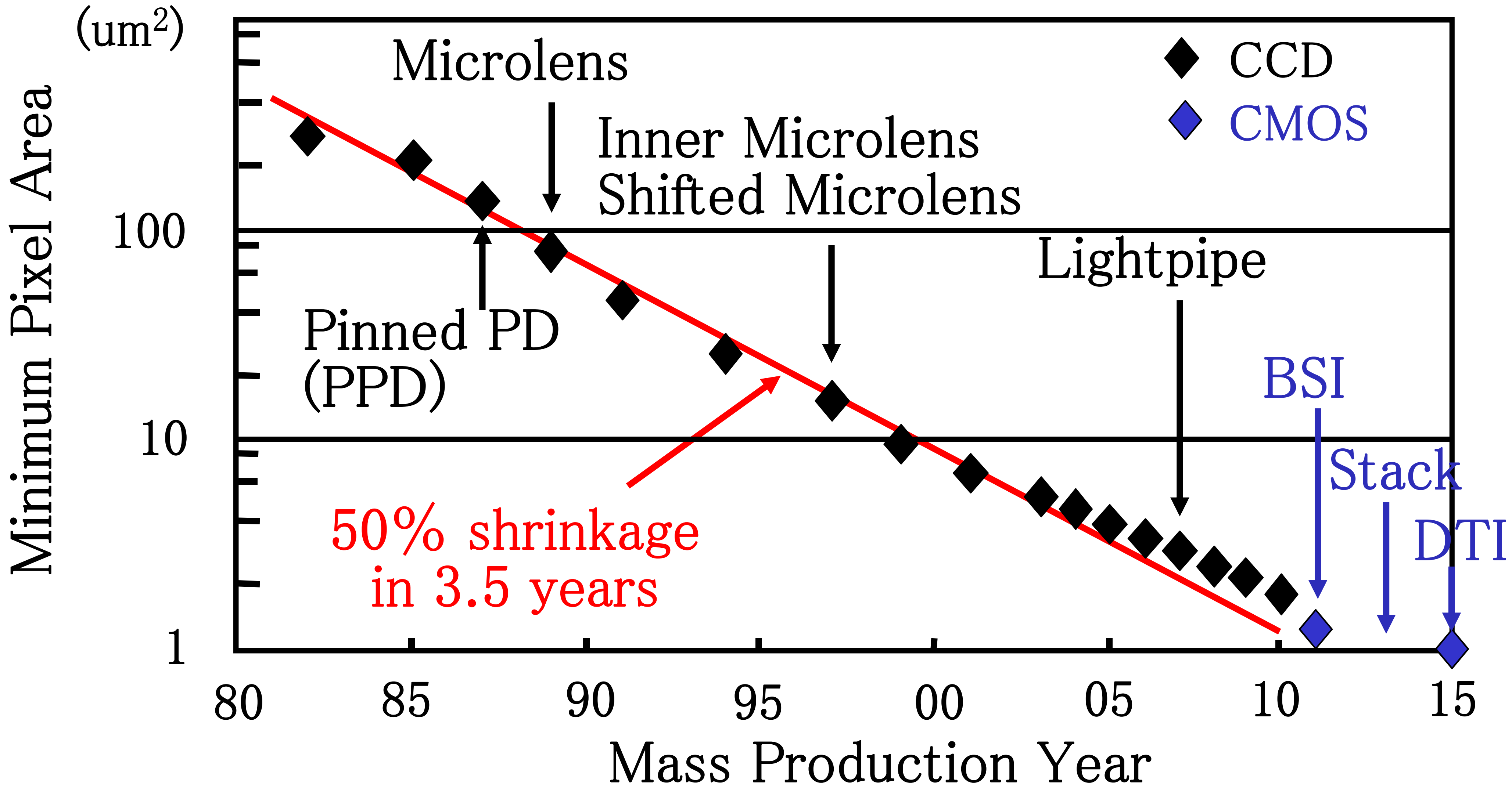


Application (2014)

(Source: TSR)

Pixel Shrinkage Trend

- Shrinkage speed becomes slower recently.
- In 2015, 1 um pixel began to be mass produced.



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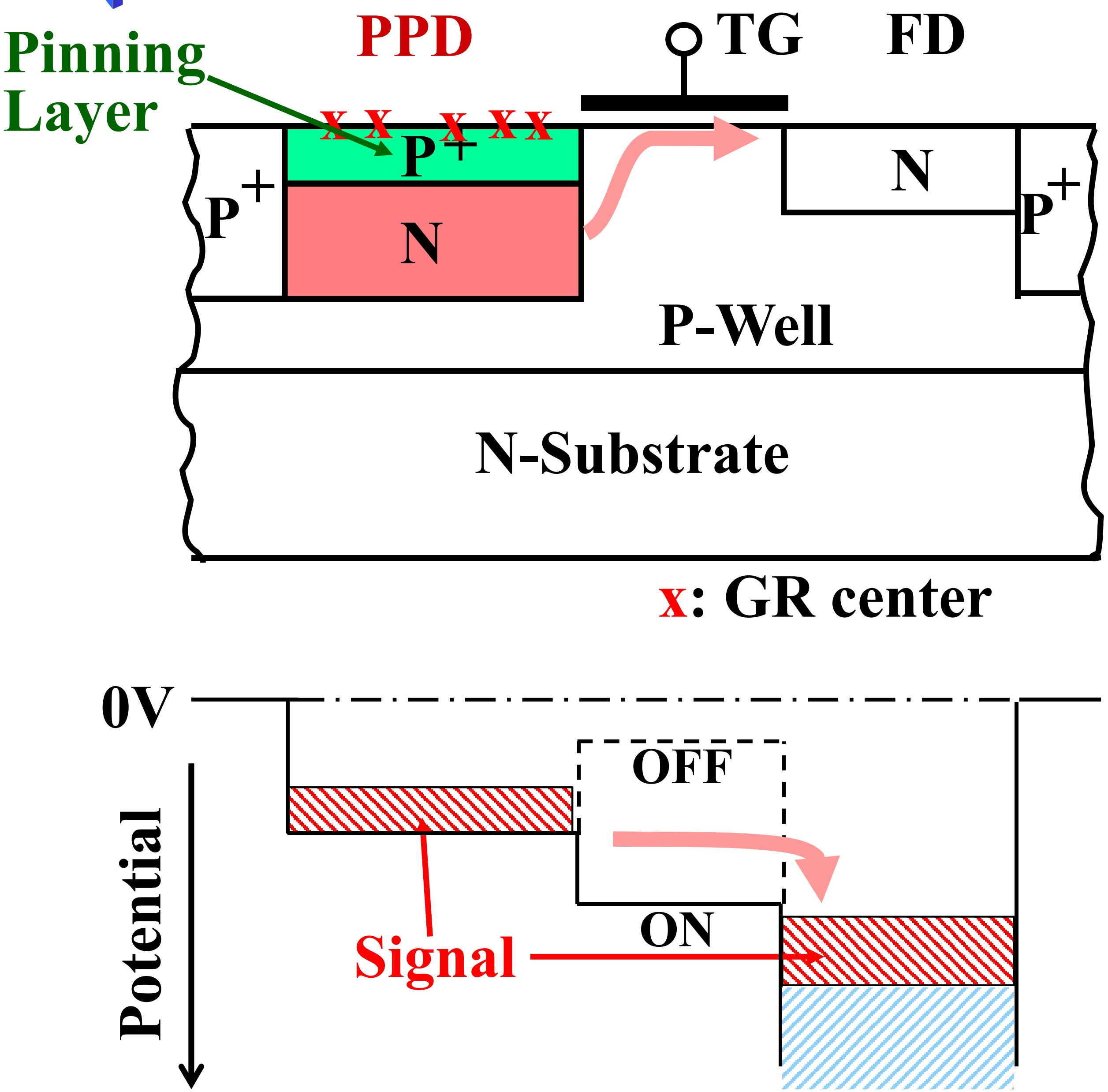
PPD Structure and Advantages



1. The P^+ pinning layer prevents the interface from being depleted, and stabilizes the PD electrically.
   - Low dark current
   - Large saturation
   - High sensitivity
   - Electronic shutter
2. Complete charge transfer
   - No image lag
   - No transfer noise

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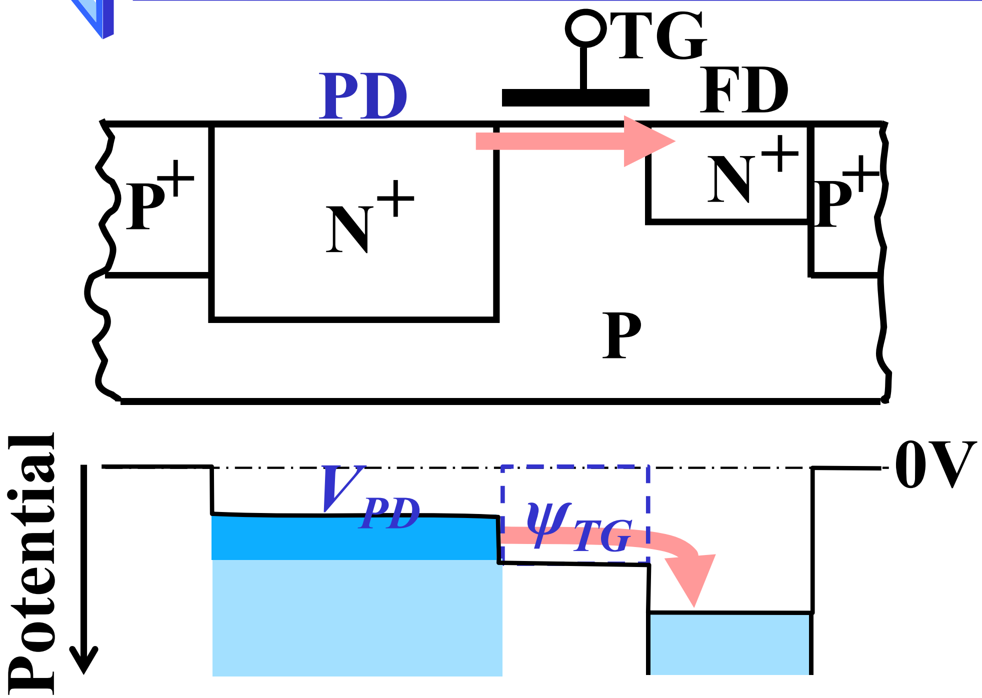
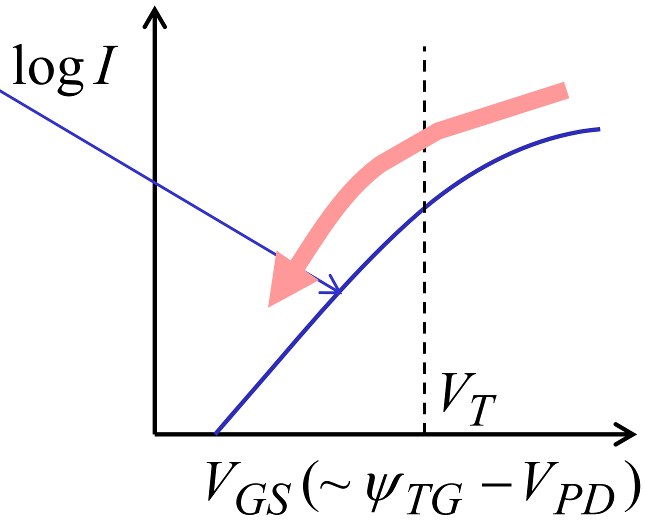
Cause of Image Lag in Conventional PN PDs (1)



Subthreshold current

$$I \sim e^{\frac{qV_{GS}}{mkT}}$$

$$(m = 1 + C_D / C_G)$$



The driving force is $\psi_{TG} - V_{PD}$, or V_{GS}.

(ψ_{TG} : TG channel potential)

Step 1. At first, TG operates in the saturation region.

Step 2. A few ns later, it enters the subthreshold region.

The subthreshold region causes image lag and transfer noise.

Causes of Image Lag in Conventional PN PDs (2)

Time evolution of V_{PD} is governed by the equation of continuity;

$$C_{PD}\frac{dV_{PD}}{dt} = I = I_0 e^{-\frac{qV_{PD}}{mkT}}$$

C_{PD}: PD capacitance
m: $1+C_D/C_G$
I_0 : constant

$V_{PD}(t)$ is derived as

$$V_{PD}(t) = \frac{mkT}{q}\ln\left\{e^{\frac{qV_{PD}(0)}{mkT}+\frac{qI_0}{mkTC_{PD}}}\right\}$$

The n[th] frame lag, $n_{lag}(n)$, is obtained with

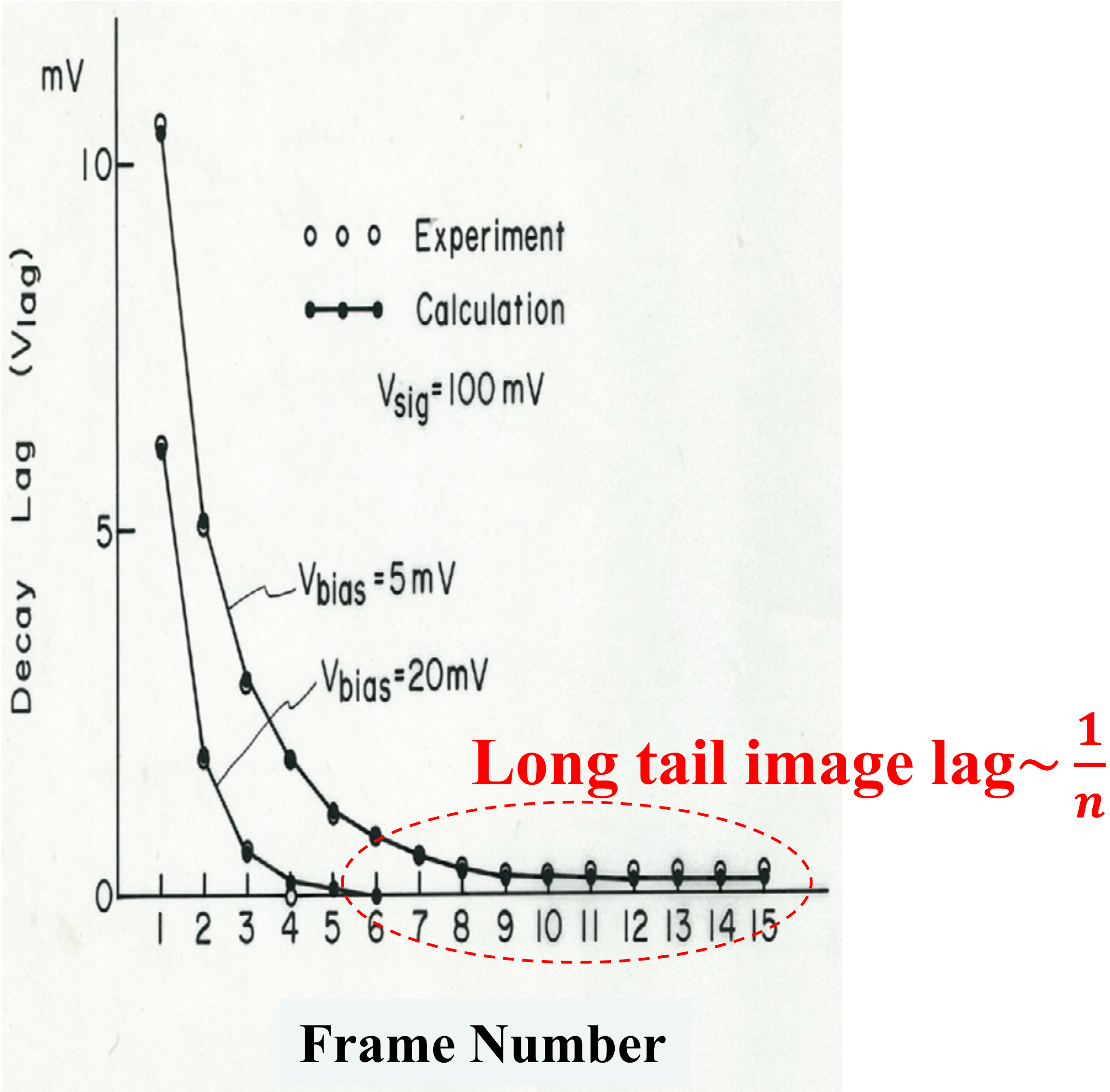
$$n_{lag}{}^{(n)} = \frac{mkTC_{PD}}{q}\ln\frac{n+1-ne^{-\frac{q^2 n_{sig}}{mkTC_{PD}}}}{n-(n-1)e^{-\frac{q^2 n_{sig}}{mkTC_{PD}}}}$$

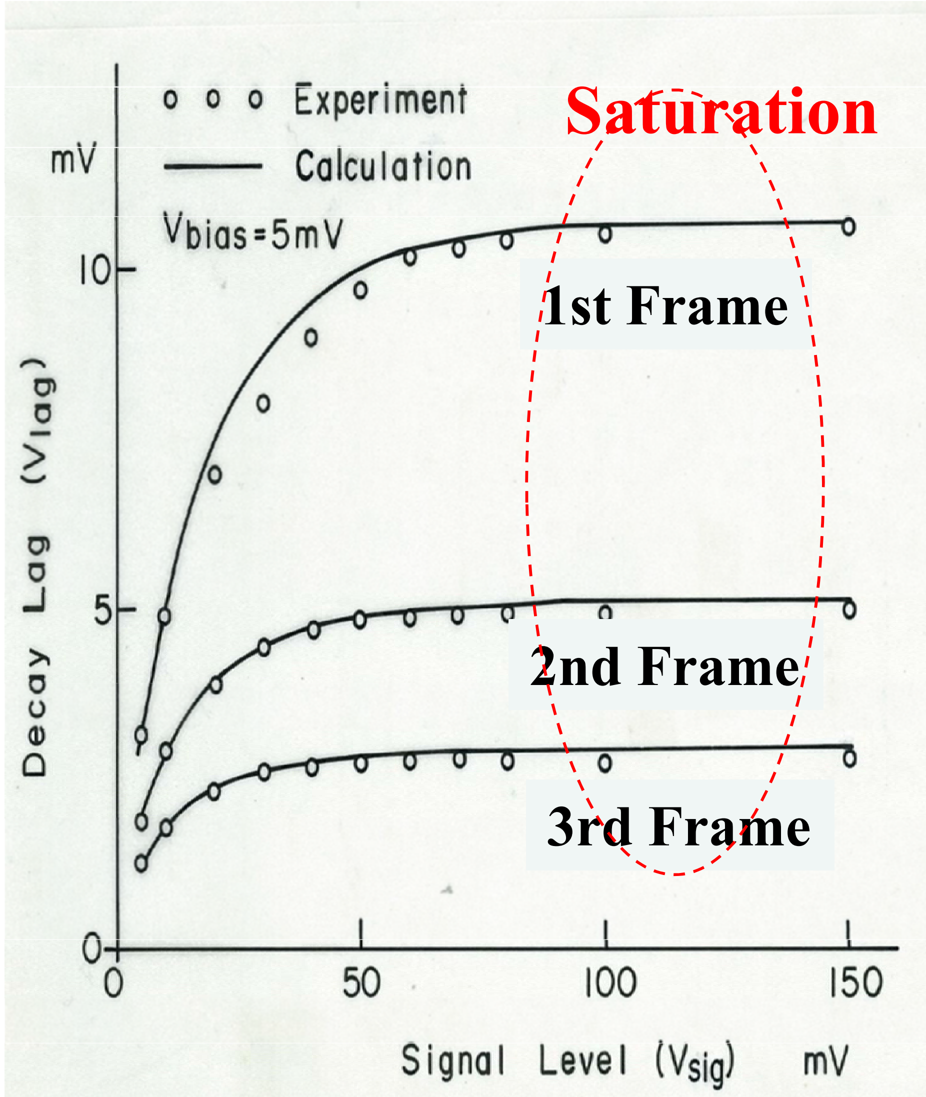
$$\sim\frac{mkTC_{PD}}{q}\frac{1}{n}$$

when n_{sig}>>1 and n>>1

(n_{sig}: signal electron number)

Image Lag in Conventional PN PDs (3)

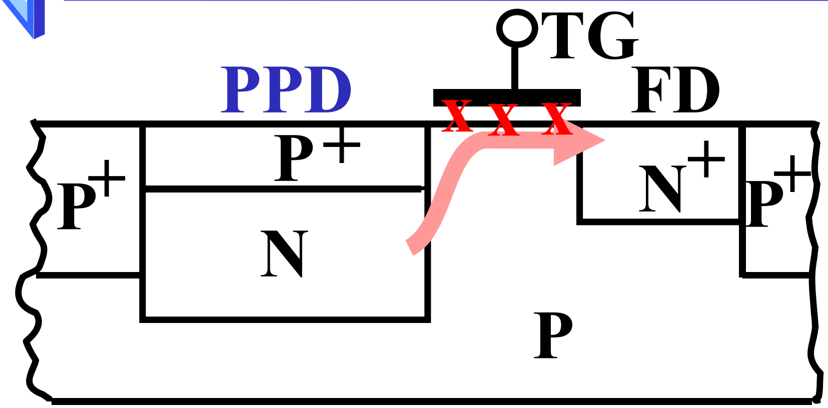


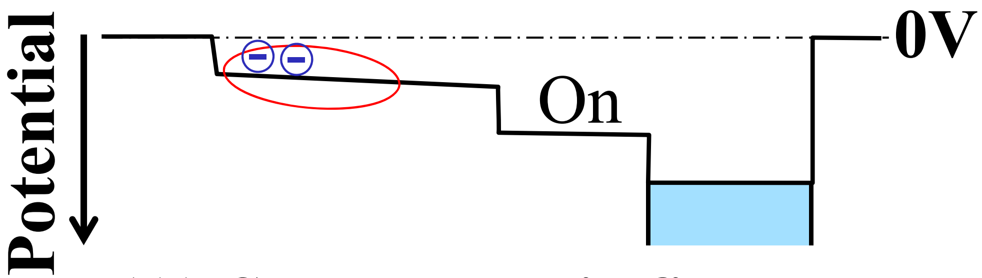


The subthreshold model matches the measurements!

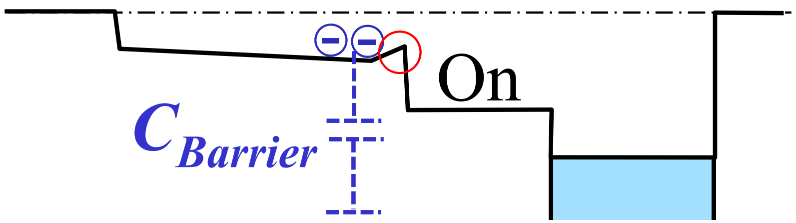
(N. Teranishi et al., IEDM, 1982)

Causes of Image Lag in PPDs (1)

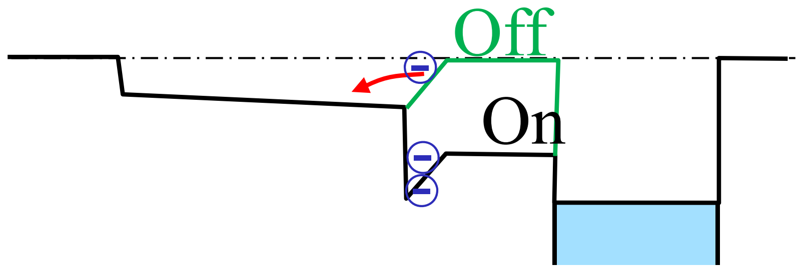




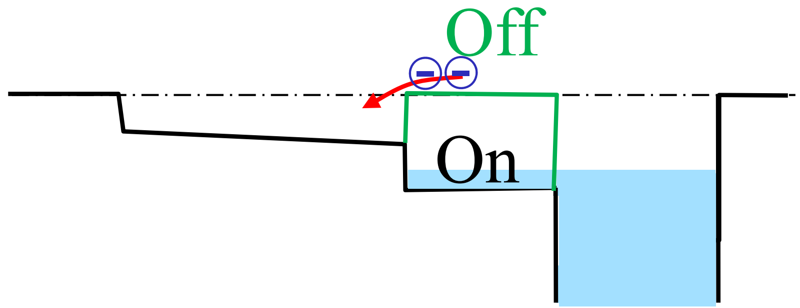
(A) Small electric field



(B) Barrier at the PD edge



(C) Pocket at the TG edge



(D) Pump back when the signal is large

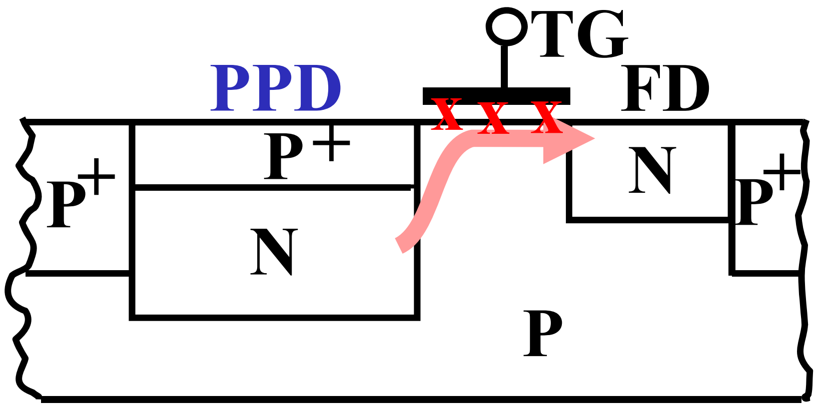
(E) Traps at the TG interface
On the next slide.

Causes of Image Lag in PPDs (2)

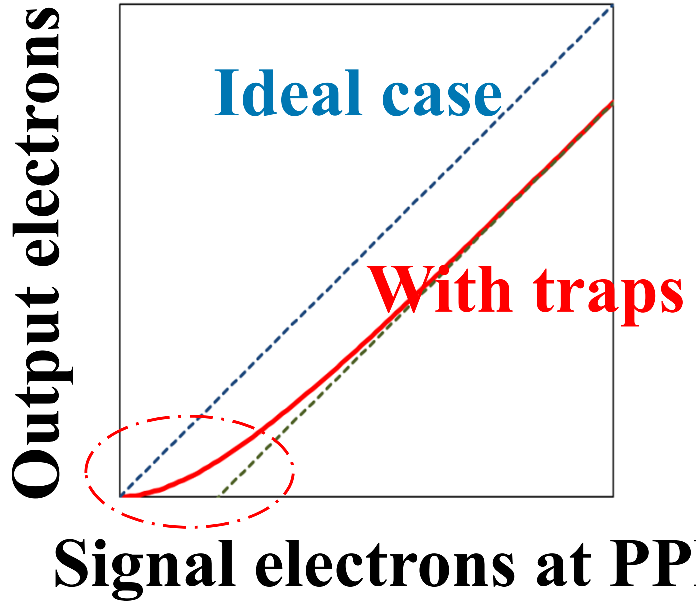
(E) Traps at the TG interface

If the electron transfer path touches the interface, some electrons are captured by traps.

- **Some of them are detrapped in the following frames, causing lag.**
- **Some of them are annihilated, causing non-linearity.**



x : Traps at the TG interface



- The signal electron annihilation exhibits this kind of non-linearity.
- A buried transfer path is needed to suppress these phenomena.

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Transfer Noise in Conventional PN PDs (1)

$$V_{PD}(t) = V_{PDa}(t) + V_n(t) \qquad (1)$$

↑ Average ↑ Noise

The equation of continuity is

$$C_{PD}\frac{dV_{PD}}{dt} = I + I_n = I_0 e^{-\frac{qV_{PD}}{mkT}} + I_n \qquad (2)$$

C_{PD}: PD capacitance
m: $1+C_D/C_G$
I_0 : constant

I_n: Noise, $\langle I_n(t_1) I_n(t_2)\rangle = qI(t_1)\delta(t_1 - t_2) \qquad (3)$

The procedure to calculate the transfer noise is

- **Step 1: Obtain $V_{PDa}(t)$.**
- **Step 2: Obtain $V_n(t)$.**
- **Step 3: Obtain the variance, $\langle V_n^2 \rangle$.**

Transfer Noise in Conventional PN PDs (2)

Transfer noise, <V_n^2>, is obtained as

$$\langle V_n{}^2 \rangle = \frac{mkT}{2C_{PD}} \frac{\frac{qI_0 t}{mkTC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}} \left(2 + \frac{qI_0 t}{mkTC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}}\right)}{\left(1 + \frac{qI_0 t}{mkTC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}}\right)^2}$$

$$+ \frac{1}{1 + \frac{qI_0 t}{mkTC_{PD}} e^{-\frac{qV_{PDa}(0)}{mkT}}} \langle V_n(0)^2 \rangle \qquad (4)$$

Not an exponential decay, and the convergence is slow.

Transfer Noise in Conventional PN PDs (3)

When $t \rightarrow \infty$, (4) becomes

$$\langle {V_n}^2 \rangle \rightarrow \frac{mkT}{2C_{PD}} \tag{5}$$

Caution:

- **This convergence is very slow, and the initial noise decay is also slow.**
- **If the TG ON period is 1 μs, we should not use this limit. We should use (4) and calculate the value at t = 1 μs, considering the initial condition.**

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Dark Current Reduction Mechanism by SRH (1)

Schockley-Read-Hall Process

$$U = \sigma v_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)} \quad (1)$$

U: Recombination Rate

(Sze: "Semiconductor Devices," Chap. 1 Eq.(59))

Assuming $\sigma_n = \sigma_p = \sigma$

1. **If depleted,** $n, p \ll n_i$

$$U = \sigma v_{th} N_t \frac{-n_i^2}{2n_i \cosh\left(\frac{E_t - E_i}{kT}\right)}$$

When $E_t = E_i$ where U is maximum, then,

$$U \approx -\sigma v_{th} N_t \frac{n_i}{2} \quad (2)$$

→ **Large dark current !**

2. **If not depleted,** $p \gg n_i \gg n$,

$$|U| \approx \left| \sigma v_{th} N_t \frac{pn - n_i^2}{p} \right| \leq \sigma v_{th} N_t \frac{n_i^2}{p} \quad (3)$$

→ **Small dark current !**

PPDs configure this non-depleted situation!

Dark Current Reduction Mechanism by SRH (2)

(1) Estimate the interface dark current reduction ratio, assuming that:

- Hole density (p) at the P^+ pinning layer: 10^{17} cm^{-3}

- Intrinsic carrier density, n_i: 1.45×10^{10} cm^{-3}

$$\frac{|U(\text{Not depleted})|}{|U(\text{Depleted})|} \leq \frac{\sigma v_{th} N_t n_i / 2}{\sigma v_{th} N_t n_i^2 / p} = \frac{p}{2n_i} \sim 10^{-7}$$

(2) Dark current comparison by image sensors.

	Non-PPD (1982)	PPD (2012)	Unit
Scheme	CCD	FSI CMOS	
Pixel size	23 x13.5	1.12 x 1.12	µm
Dark current	1,300	5.6	e^-/s/µm^2 at 60℃

0.4 %

Example of Dark Current Reduction (1)

If the dark current is reduced, the dark current FPN and dark current shot noise will also be reduced.

Conventional PD

PPD

The dark current FPN is suppressed, therefore, picture quality is much improved.

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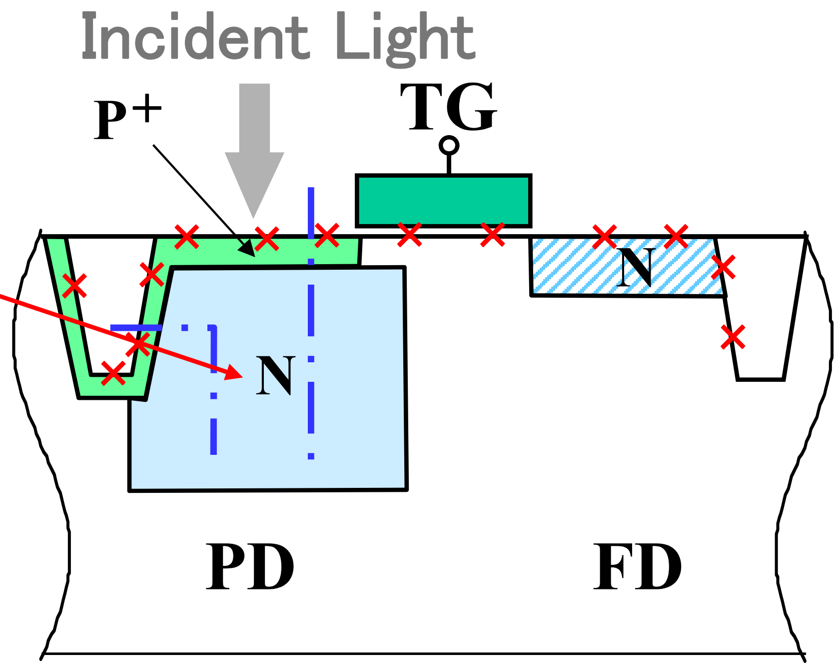
A Question About the Dark Current Reduction Mechanism

The N-type PD is depleted.



4Tr CMOS Sensor Cross Section

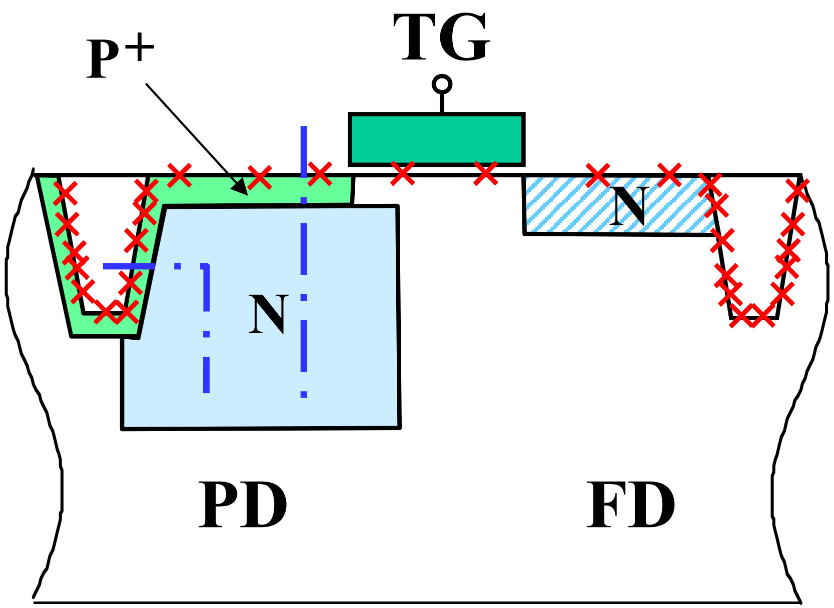
Even if the P+ pinning layer neutralizes the interface states, the N-type PD is still depleted nearby the P+ pinning layer.
The assumption of "spatial uniformity," which is implicitly used in SRH, is not realistic!

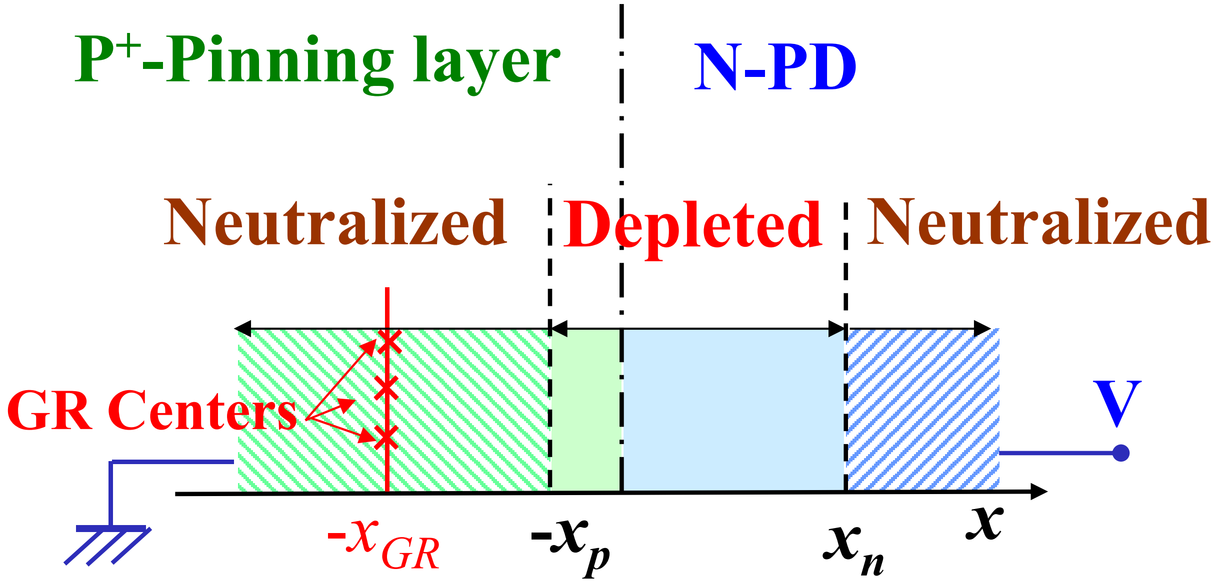
To understand the effects and limitations of PPDs, a new, correct model is needed.

A New Model Including Non-Spatial-Uniformity

Modified Diffusion Current Model:

- 1-Dim (Along — · — · — ·)
- Put the GR centers at $x = -x_{GR}$ in the neutralized region.
- Assume still "stationarity," but no more "spatial uniformity."
- No electric field in the neutralized region. Low injection.
- Use the same notation of Sze's "Semiconductor Devices."





New Model

New Diffusion Current Model with GR Center

Introduce the GR centers' effect into the diffusion equation:

$$D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} - GD_n(n_p - n_{p0})\delta(x + x_{GR}) = 0 \qquad (3)$$

- At $x = -x_{GR}$, the GR centers force n_p toward n_{p0}, the equilibrium.
- G: Intensity of the GR Centers. Unit is 1/cm.

  GL_n is a dimensionless parameter for the GR centers' intensity.

  $L_n \equiv \sqrt{D_n \tau_n}$: Diffusion Length

Boundary Conditions:

- Same as in the diffusion current model without GR centers

$$n_p = n_{p0} \quad \text{at} \quad x = -\infty \qquad (4)$$

$$n_p = n_{p0} e^{qV/kT} \quad \text{at} \quad x = -x_p \qquad (5)$$

Derived Solution

Diffusion Current (Dark Current) with GR Centers

$$J_n^{(GR)}(-x_p) = J_n^{(0)}(-x_p) \times EDCF \qquad (6)$$

where

$$J_n^{(0)}(-x_p) \equiv \frac{qD_n n_{p0}}{L_n}(e^{qV/kT} - 1) \qquad (7)$$

Diffusion Current (Dark Current) without GR Centers

$$EDCF \equiv \frac{GL_n + 1}{GL_n + 1 - GL_n e^{-(x_{GR} - x_p)/L_n}} \qquad (8)$$

***EDCF*: Extra Dark Current Factor**

$L_n \equiv \sqrt{D_n \tau_n}$ **: Diffusion Length**

GL_n**: Dimensionless Parameter for the GR Centers' Strength**

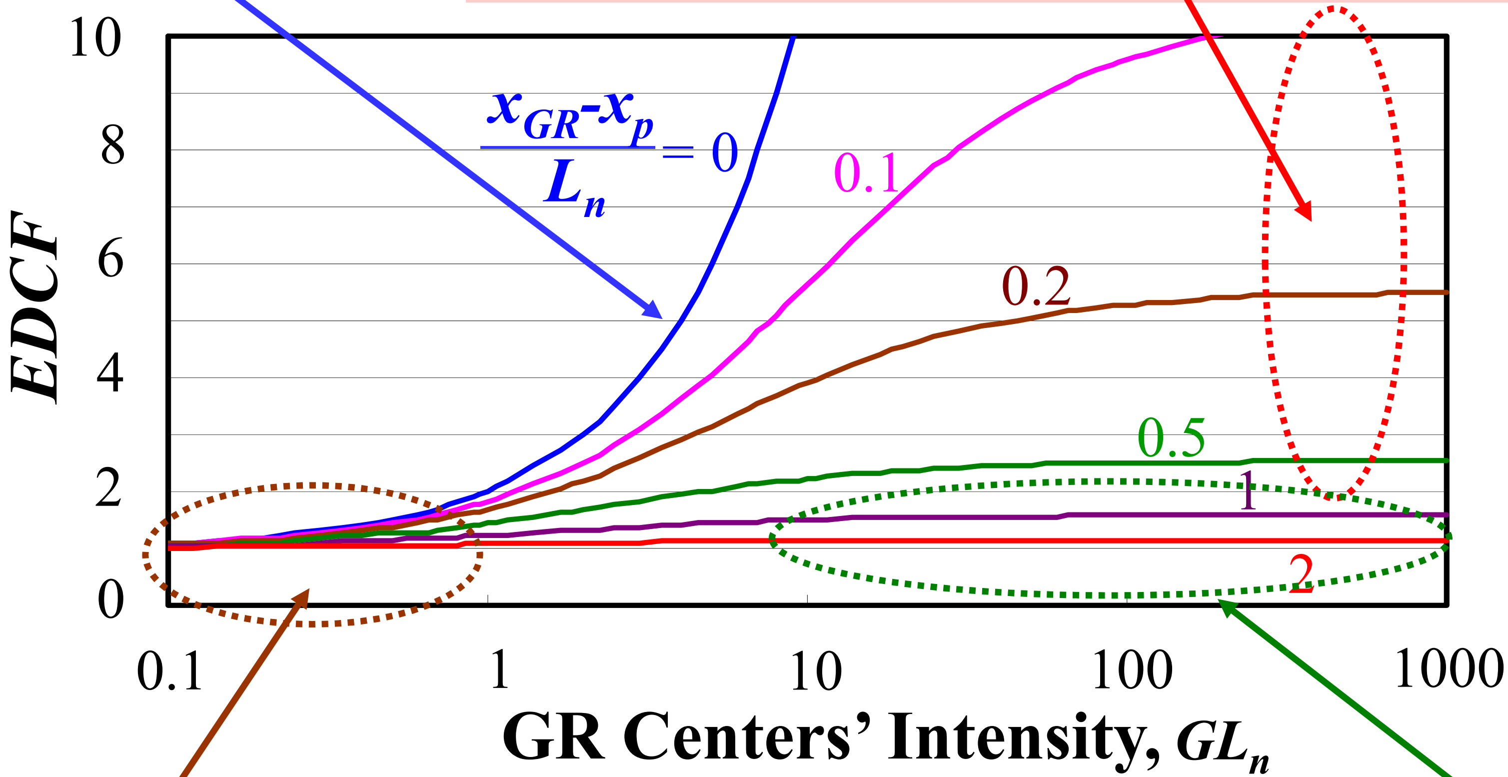
Characteristics of the New Diffusion Current Model

When $(x_{GR} - x_p)/L_n = 0$, GR centers become not neutral; $EDCF = GL_n + 1$

When $GL_n \to \infty$, then, $EDCF \to \dfrac{1}{1 - e^{-(x_{GR}-x_p)/L_n}}$

No divergence; instead, saturation.

Temperature dependence: $J_n^{(GR)} \propto J_n^{(0)} \propto e^{E_g/kT}$

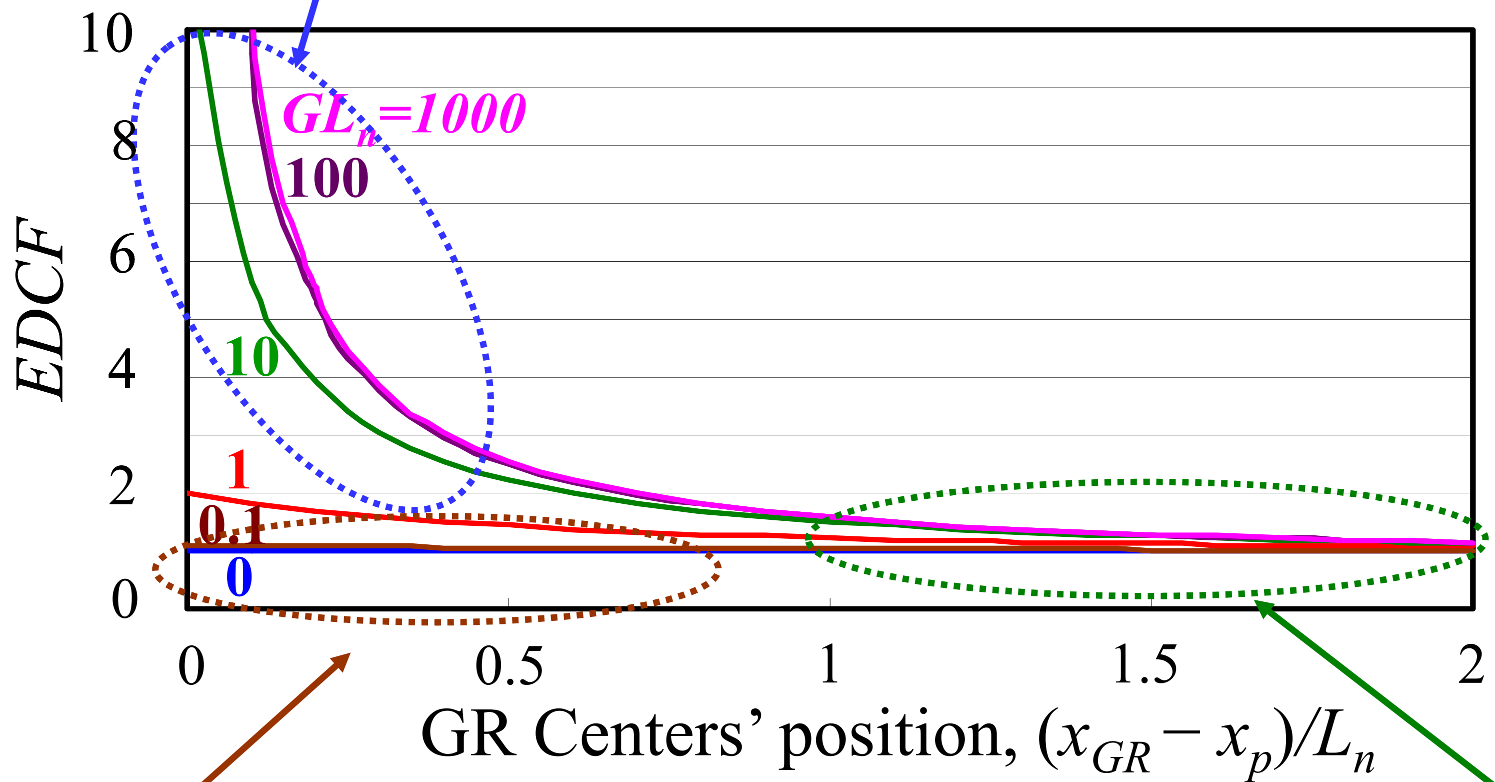


When $GL_n \to 0$, $J_n^{(GR)} \to J_n^{(0)}$
Reasonable.

When $(x_{GR} - x_p)/L_n \to \infty$, $EDCF \to 1$.
The GR centers' effect becomes negligible.

Characteristics of New Diffusion Current Model (2)

When $(x_{GR} - x_p)/L_n \rightarrow 0$, *EDCF* increases, because the GR centers' position approaches the depletion region.



When $GL_n \rightarrow 0$, $J_n^{(GR)} \rightarrow J_n^{(0)}$

Reasonable.

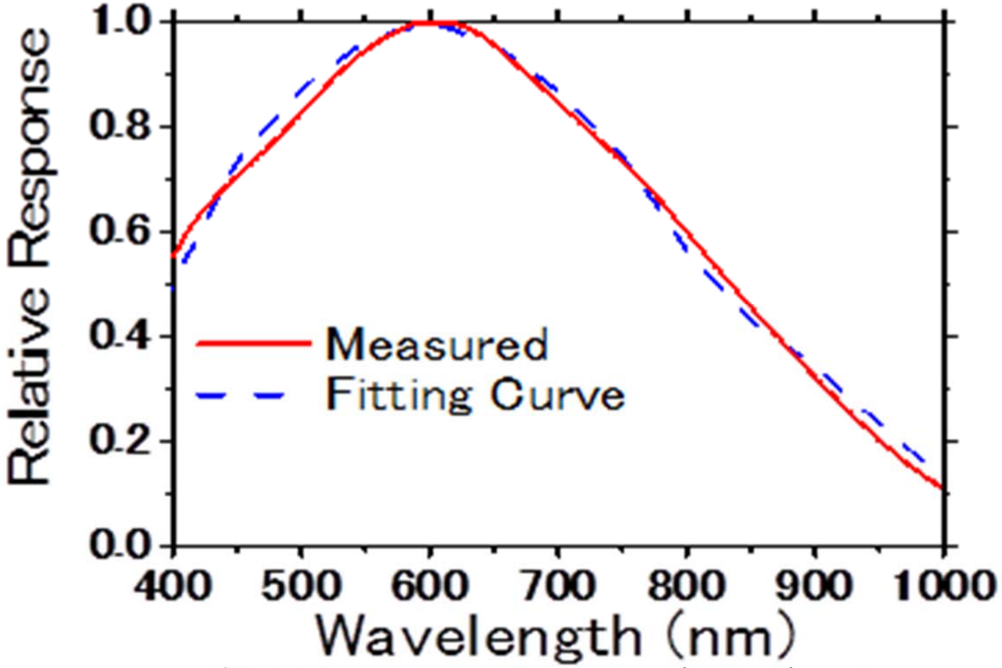
When $(x_{GR} - x_p)/L_n \rightarrow \infty$, $EDCF \rightarrow 1$.

The GR centers' effect becomes negligible.

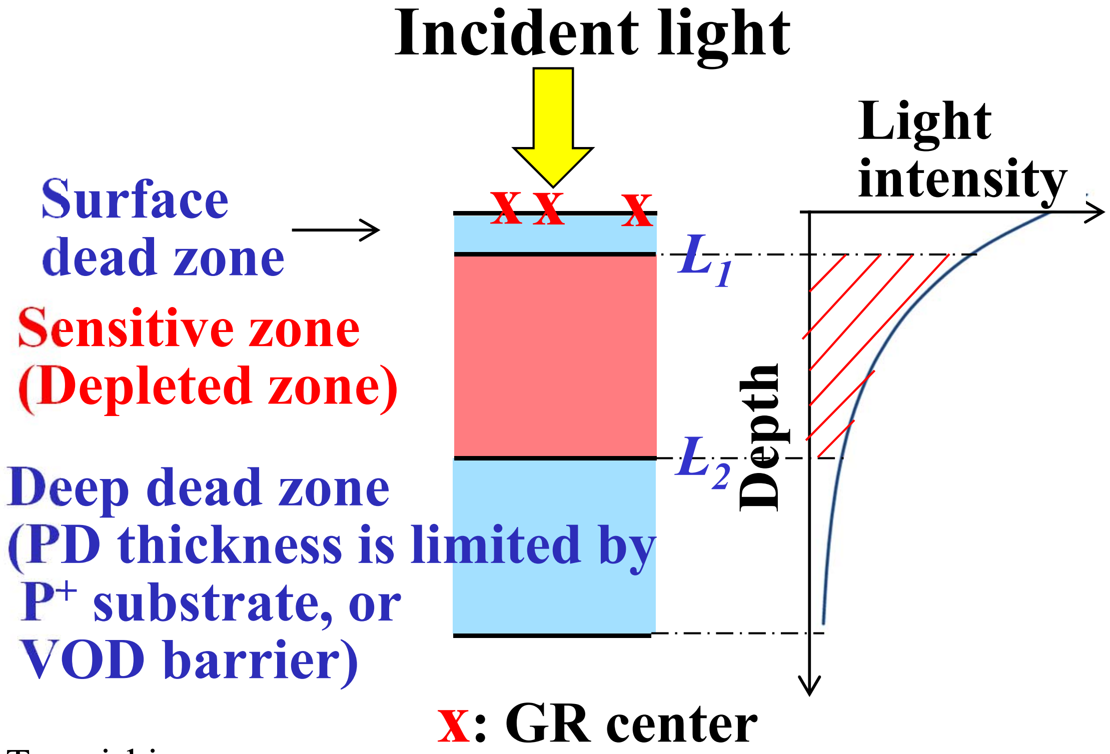
Is the P^+ Pinning Layer Thickness Sufficient?

- How large is the diffusion length, L_n, in the P^+ pinning layer?
- The surface dead zone depth, L_1, might be a good alternative for L_n.
- L_1 is derived from the spectral response, to be ~0.08 μm.
- P^+ pinning layer thickness ≈ 0.05 – 0.5 μm

The GR centers at the silicon surface possibly contribute to the dark current! We should reduce the GR centers.



(SONY ICX658ALA data sheet
Pixel size: 6.35 x 7.4 um)



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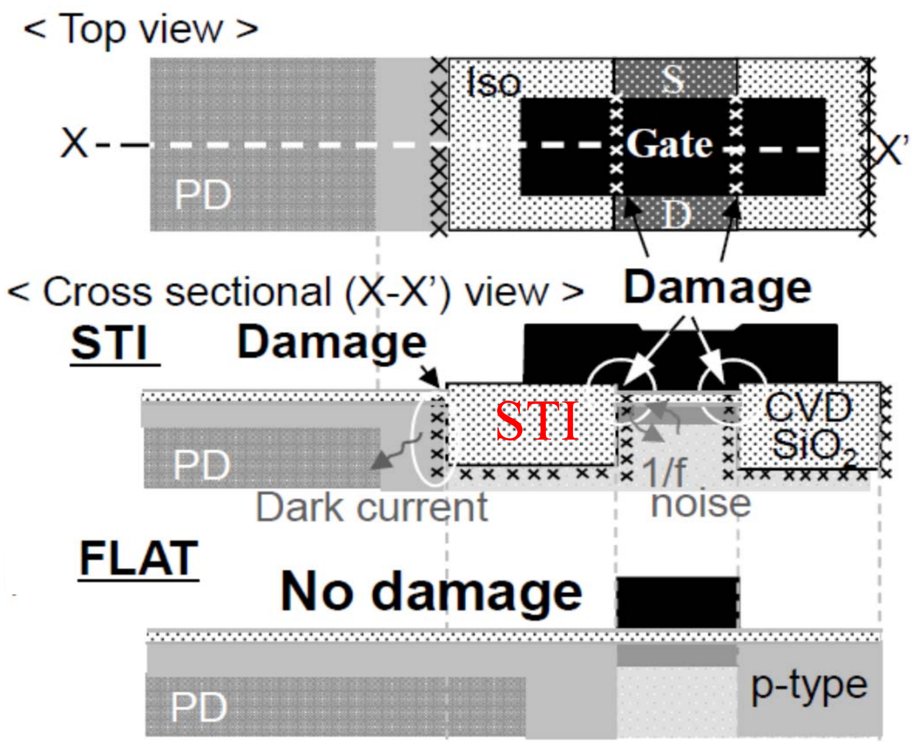
Macroscopically Flattening

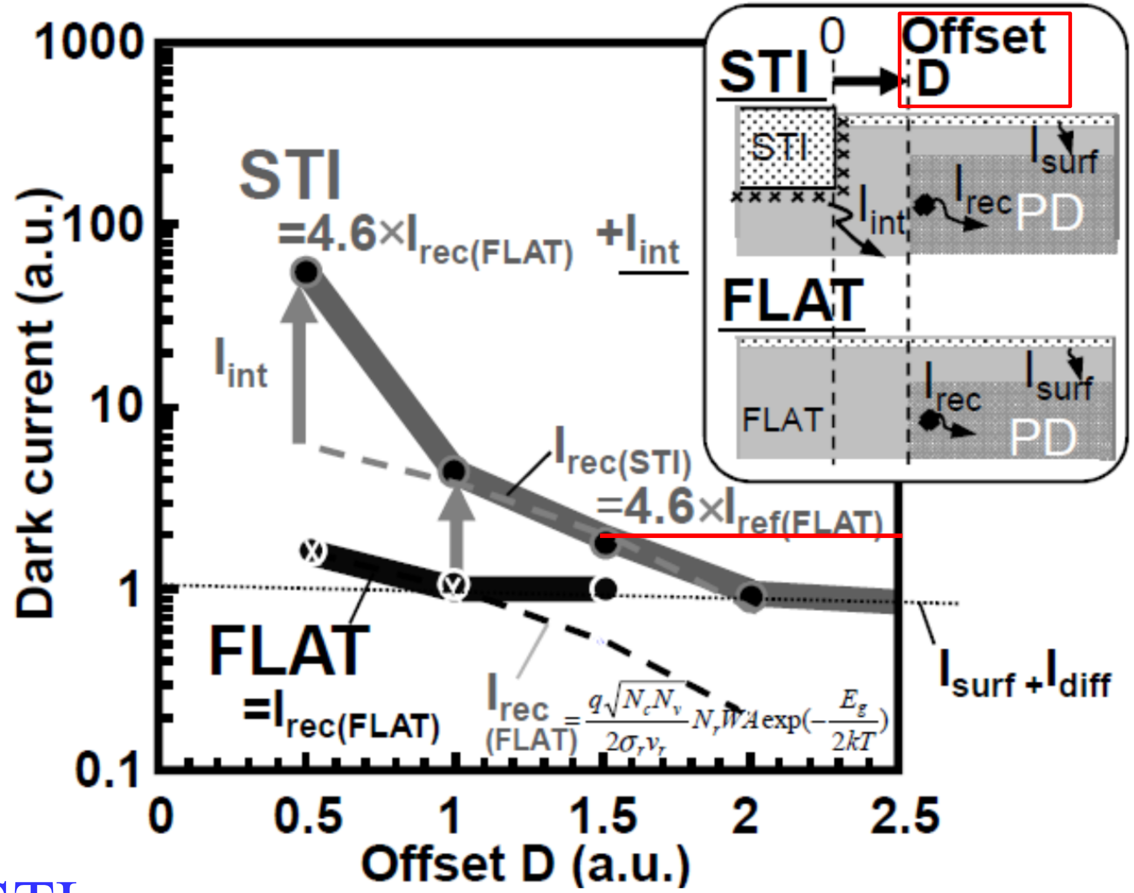
Itonaga et al. (Sony), IEEE IEDM, 2011

No isolation grooves/ridges and no substrate etching as in STI

➡ **Less process damage, less stress and no STI side surface.**



Structure of “FLAT,” comparing with STI

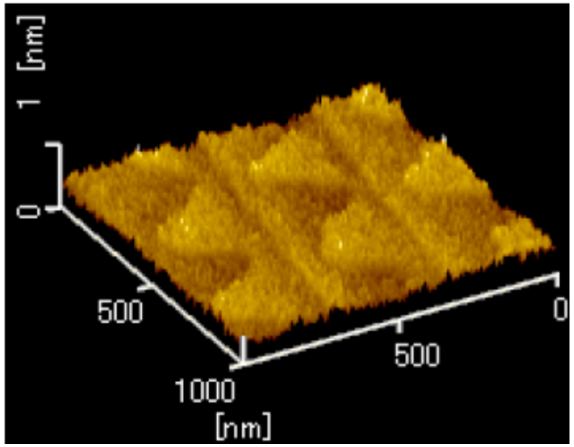


$I_{rec(FLAT)} = \frac{q\sqrt{N_c N_v}}{2\sigma_r v_t} N_t W A \exp(-\frac{E_g}{2kT})$

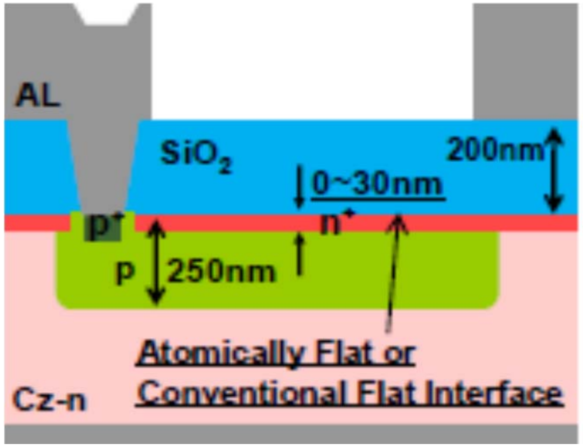
Dark Current

Atomically Flattening

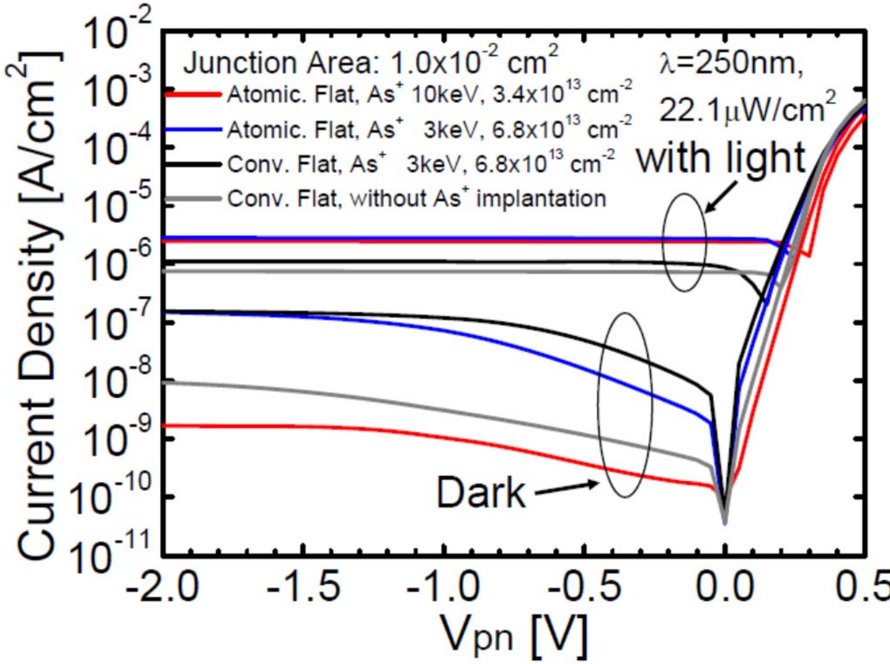
Kuroda et al. (Tohoku Univ.); “Highly Ultraviolet Light Sensitive and High Reliable Photodiode with Atomically Flat Si Surface”

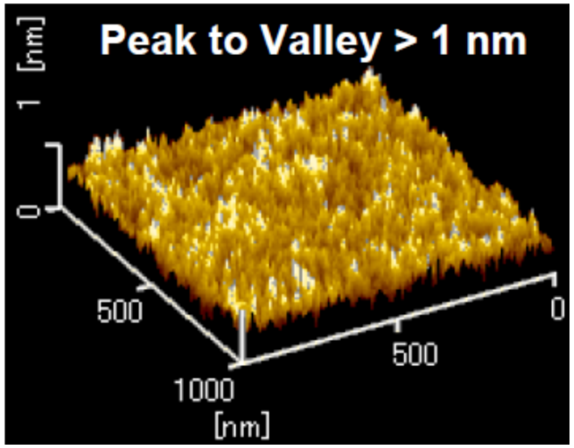


Atomically Flat (100).
Atomic step is 0.135nm.



N⁺PN PD





- **Low Dark Current, High QE for UV at PD.**
- **Low 1/f noise at MOS Tr.**

▪ **Atomically flat surfaces reduce GR centers/traps.**

Typical (100) after RCA Cleaning.

AFM Images

Contents

Vertical Overflow Drain (VOD) Shutter

For Anti-blooming and electronic shutter

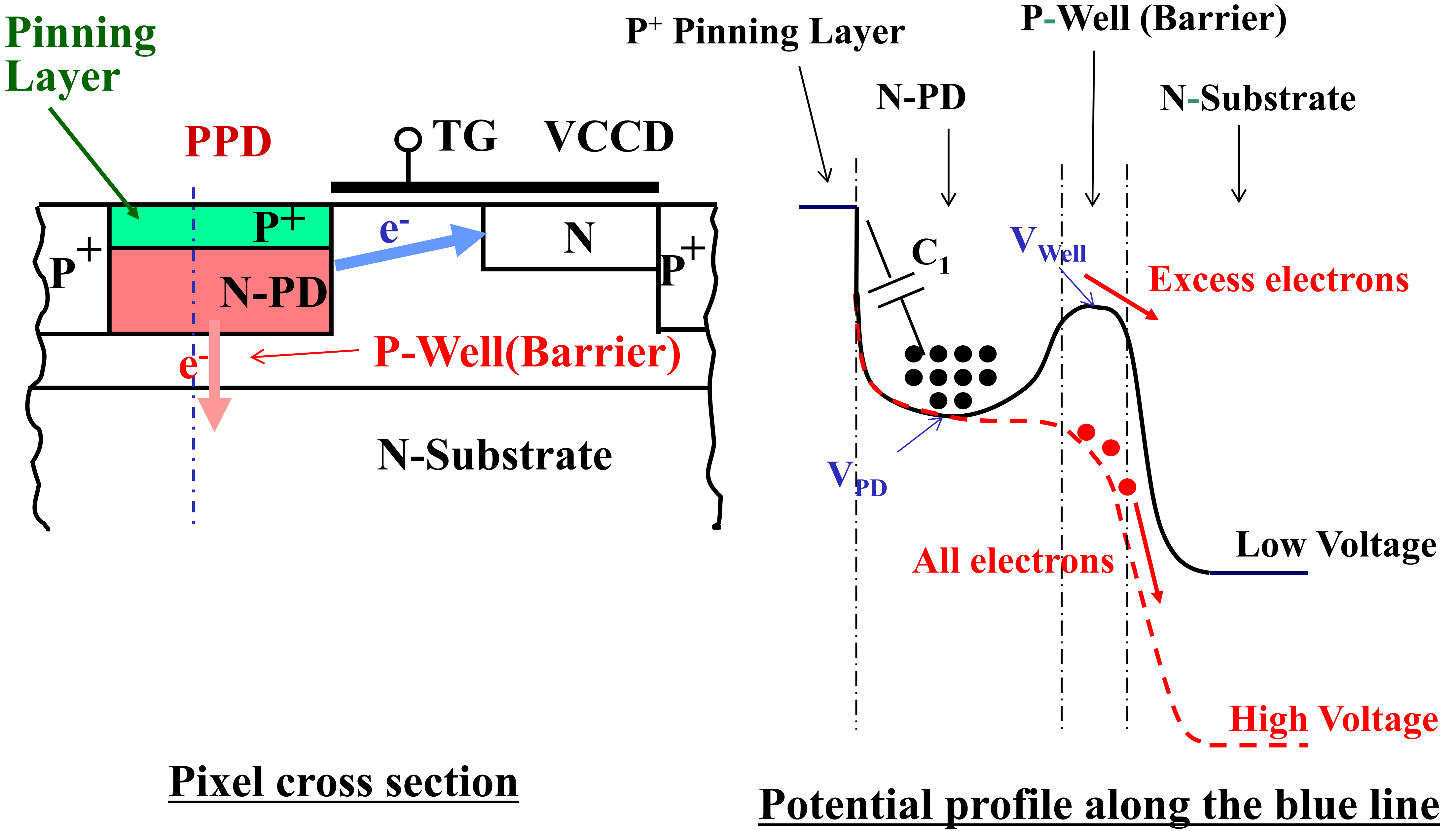
- **The VOD is used in CCD image sensors**
- **TG is used as LOD (lateral overflow drain) in CMOS image sensors.**

Blooming

Electronic Shutter

(Object is rotating at 720 rpm.)

VOD Structure and Mechanism



High Speed Shutter (1)

Definitions

- **High speed shutter**: Short exposure time / sharp shutter
- **High speed camera**: High frame rate

Motivations of high speed shutter

- High speed motion capture, ToF, fluorescence life time imaging.
- Replace the streak tube and gated image intensifier.

Shutter speed is limited by:

(1) Photo-generated carrier collection time into the PD storage region.

(2) Driving pulse delivery time, $C \times R$.

(3) Carrier transferring time from the PD storage to analogue memory in the pixel.

- The VOD shutter mechanism with PPD has a merit on item (2).

High Speed Shutter (2) --- Load Capacitance ---

VOD shutter

- **Substrate capacitance**

$$C_{Sub} = \frac{K_{\mathrm{Si}}\varepsilon_0 S}{d}$$

where,

K_{Si}: Si dielectric constant

ε_0: Permittivity in vacuum

S: Area,

d: distance (depletion thickness)

For example, 1/3 inch

$S = 28\ \mathrm{mm}^2$

$d = 7.5\ \mu\mathrm{m}$

$C_{sub} = 400\ \mathrm{pF}$

LOD shutter

- **Gate capacitance, C_{gate}, + parasitic capacitance of wires, C_{wire}**

$$C_{Gate} = N_{\mathrm{pixel}} \frac{K_{\mathrm{SiO2}}\ \varepsilon_0 WL}{t}$$

where, N_{pixel}: Pixel number

K_{sio_2}: SiO_2 dielectric constant

W: Channel width,

L: Channel length,

t: Gate SiO_2 thickness

For example, $N_{\mathrm{pixel}} = 1.3$ M,

$W = L = 0.4\ \mu\mathrm{m}$, $t = 6$ nm

$C_{Gate} = 1{,}200\ \mathrm{pF}$

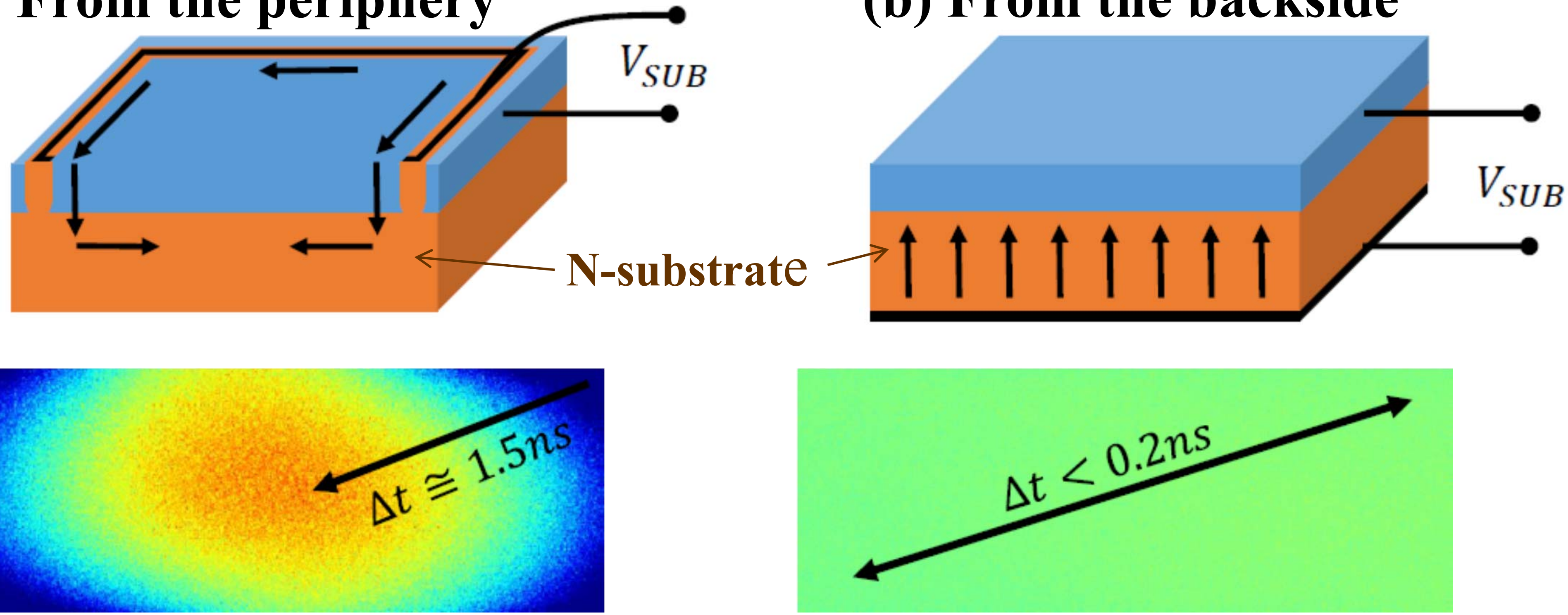
$C_{Wire} = ?$

The load capacitance of the VOD shutter is smaller than that of the LOD shutter.

High Speed Shutter (3) --- Parasitic Resistance

Two methods for driving pulse delivery:

(a) From the periphery **(b) From the backside**



- **A small parasitic resistance and small variations of the parasitic resistance are achieved with (b) backside feeding.**
- **A skew smaller than the measurement accuracy limit (0.2 ns).**

(E. Tadmor et al., 2014 IEEE Sensors)

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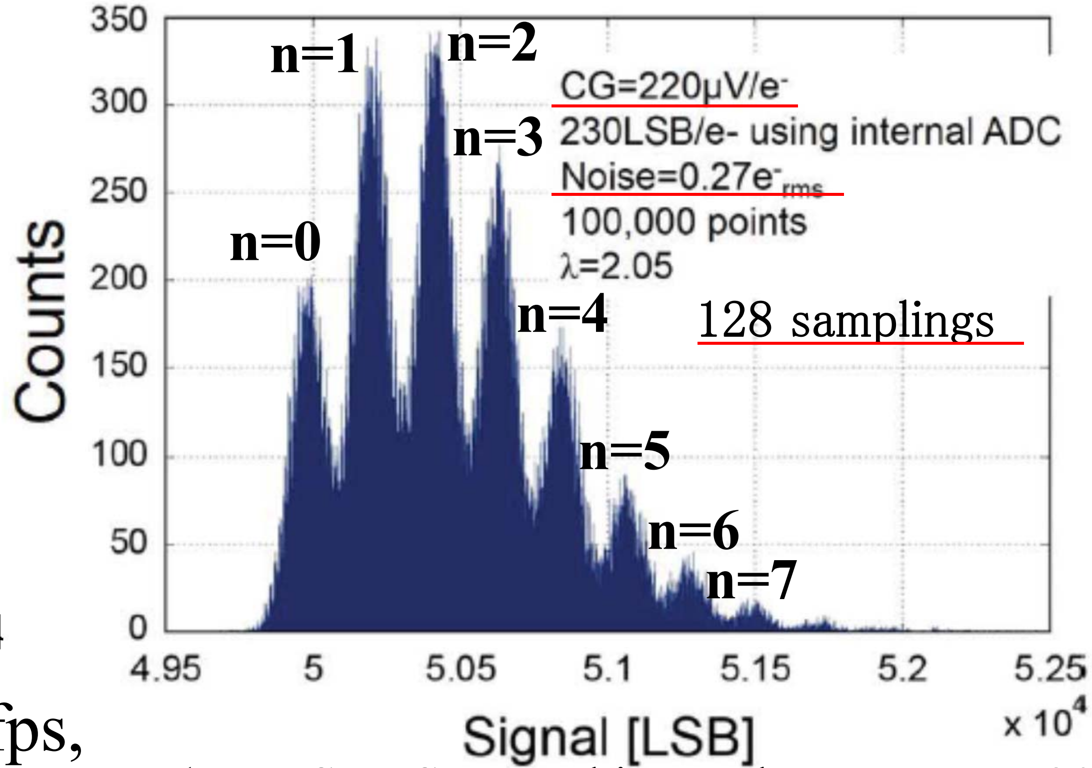
Visible Light Photon Counting Image Sensor

SPAD
(Single photon avalanche diode)

(N. Dutton et al., VLSI Symposium 2014

- QVGA (320x240 pixel) SPAD, 20 fps, at room temperature, at night
- High avalanche gain makes following circuit noise negligible.
- Large dark count. Small fill factor

4-Tr CMOS + High conversion gain + CMS (Correlated multiple sampling)



(MW. Seo, S. Kawahito et al., IEEE EDL 2015)

- In 2015, several organization reported low noise < 0.3 e- rms.

ref. DEPFET (Max Plank) uses CMS.

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Conclusion

1. The PPD is a primary technology for CCD and CMOS image sensors. It exhibits low noise, low dark current, no image lag, large saturation, high sensitivity, and allows electronic shutter operation.

2. Conventional non-PPDs have long tail lag and transfer noise.

3. A new diffusion dark current model considering the GR centers is proposed. If the P+ pinning layer is thin compared with diffusion length, they contribute to the dark current.
 The temperature dependence is $J_n^{(GR)} \propto e^{E_g / kT}$.

4. Both macroscopiccally and atomically flatness of the silicon surface reduce the dark current.

5. VOD shutters with PPDs are capable of high speed shutter operation.