Radiation Tolerance of 65nm CMOS Transistors

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Abstract

We report on the effects of ionizing radiation on 65nm CMOS transistors held at approximately $-20°C$ during irradiation. The pattern of damage observed after a total dose of 1 Grad is similar to damage reported in room temperature exposures, but we observe less damage than was observed at room temperature.

Keywords:
PACS:

1. Introduction

The need for extremely radiation tolerant electronics is one of the major issues confronting high energy physics in the era of High Luminosity running at the CERN Large Hadron Collider (HL-LHC). Tests at CERN [1], published in 2012, established 65nm CMOS as the leading candidate technology for HL-LHC electronics. Using an X-ray beam, Bonacini, *et al.* exposed 65nm transistors to a total dose of 200 Mrad. Their results showed, with one exception, relatively small changes in transistor parameters for normal layout standard gate oxide thickness (core) transistors. The exception was a dramatic loss of maximum drain-source current in the narrowest PMOS transistors. The CERN group concluded that 65nm CMOS technology can be used for HL-LHC applications with no special design considerations, except that all core devices should have width greater than 360nm.

The RD53 collaboration was formed in 2014 to further explore the feasibility of using 65nm CMOS technology to design a pixel readout chip for use at the HL-LHC [2]. The group established a total ionizing dose tolerance goal of 1 Grad. The measurements reported in this paper were done in the context of RD53. Discussions late in 2013 within RD53 centered on the fact that the data presented in reference [1], and also subsequent data collected by the CERN group and by a group from CPPM [3], contain evidence of significant room temperature annealing during the time between X-ray exposures. Both CMS and ATLAS currently plan to operate their HL-LHC pixel vertex detectors at

approximately $-20\,^{\circ}$C. This is because the silicon strip trackers will operate at $-20\,^{\circ}$C in order to limit leakage current in the silicon sensors, which would otherwise require much more cooling and therefore more mass in the tracking volume. Concern was expressed that 65nm circuits might experience greater radiation damage than had been observed in room temperature exposures if they were maintained at $-20\,^{\circ}$C during irradiation.

We report the results of an irradiation of 65nm transistors performed using the Gamma Irradiation Facility at Sandia National Laboratory [4]. The devices under test were maintained at a temperature $\lesssim -20\,^{\circ}$C during irradiation.

2. Apparatus and Technique

2.1. Test ASIC

A 65nm CMOS Application Specific Integrated Circuit (ASIC) containing individual transistors connected to wire bond pads was designed at Fermilab and fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC)[1]. The test ASIC was part of a multi project wafer submitted to TSMC through the Metal Oxide Semiconductor Implementation Service (MOSIS)[2]. The chip was divided into two parts, one part intended primarily for lifetime studies of devices operated at liquid argon temperature, and one part intended for radiation tolerance testing. Table 1 lists the transistors that were tested in this study. Most of the core transistor varieties available in the TSMC 65nm CMOS process are represented. As indicated in the table, there are five groups of similar transistors. Within a group, all transistors share a diode-protected gate pad, and an (unprotected) source pad. The drain of every transistor is connected to its own wire bonding pad. We tested PMOS and NMOS core (1.2V) transistors, and NMOS I/O (2.5V) transistors (with double thickness gate oxide).

2.2. ASIC package, test equipment, and measurement procedures

The test ASICs were wire bonded into pin grid array chip carriers so that they could be irradiated on simple printed circuit boards (PCBs) containing no active components other than the test ASICs, and tested on more complicated PCBs. Transistor characteristics were measured with the chip carriers mounted on boards containing switches that allowed individual transistors to be measured one at a time. The number of pads on the test ASICs was too large to allow all pads to be wire bonded in one package, given the chosen chip carrier, so three different packages with different wire bonding patterns were made. One package had bonds only to devices intended for cold tests. NMOS transistors were wire bonded in the second package, and PMOS transistors were wire bonded in the third package. The devices intended for cold tests are all large transistors

[1] Our test chip was fabricated at TSMC fab 14. The devices tested earlier at CERN were fabricated at TSMC fab 12 [5].

[2] MOSIS is operated by the Information Sciences Institute at the University of Southern California.

Standard PMOS Gate 1	120/60, 360/60, 600/60, 1000/60
Standard PMOS Gate 2	5000/500, 5000/5000
Standard NMOS Gate 1	120/60, 240/60, 360/60, 480/60, 600/60, 1000/60
Standard NMOS Gate 2	5000/500, 5000/5000, ELT 2050/60, zV_{th} 1500/300, zV_{th} ELT 2240/300, TW 120/60, TW 5000/60
Double Gate Oxide Thickness NMOS	400/280, 500/280, 800/280, 1000/280, 5000/500, 5000/5000, ELT 2220/280, zV_{th} 3380/1200, TW 400/280, TW 800/280, zV_{th} ELT 3450/1200

Table 1: Transistors tested in this study: The numbers indicate transistor size (W/L = channel Width/Length in nm), ELT indicates an Enclosed Layout Transistor, zV_{th} indicates a transistor with threshold voltage = 0, and TW indicates Triple Well NMOS transistors laid out with the Pwell within a deep Nwell.

unlikely to be used in a pixel readout ASIC. They have been excluded from this analysis.

A different PCB was used to test each ASIC package. These test PCBs were connected to two Keithley 237 Source Measurement Units (SMUs) using triax cables and to a National Instruments USB-6501 I/O board by a twisted-pair ribbon cable. The I/O board was connected to a USB port of a laptop computer running Labview. Bias voltage for the protection diodes was generated by a voltage regulator on the test PCB from the 5V provided by the laptop USB port. The Labview program controlled solid state switches on the test PCB that connected one of the SMUs to a single gate pad at a time; unused gates were grounded. The program controlled LEDs on the test PCB to indicate how mechanical (rotary) switches on the test PCB should be set to connect the other SMU to a single transistor drain. All three voltage sources were referenced to a common ground plane on the test PCB, and the source pads for all transistors in a package were connected directly to this ground. The fact that we did not separate the return current path for the two SMUs, together with possible parasitic circuits involving the protection diodes and the solid state switches in the OFF state, made it impossible for us to accurately measure the leakage current of transistors in the ASIC packages.

2.3. Irradiation

The Sandia National Laboratory Gamma Irradiation Facility (GIF) uses ^{60}Co sources to provide controlled doses of ionizing radiation. ^{60}Co decays by beta decay to an excited state of ^{60}Ni. The ^{60}Ni relaxes to the ground state by emitting two gamma rays of energy 1.17 and 1.33 MeV [6]. At the Sandia GIF, ^{60}Co is held in stainless steel "source pins" that are 3/8 inch diameter

and 18 inches long. A number of source pins are mounted in an array and to first order, none of the beta electrons escapes the steel source pins. When not in use, the sources are kept at the bottom of an 18 foot deep pool of deionized water which provides shielding. The facility has three shielded irradiation cells in a single high bay area above the shielding pool. Each irradiation cell has an opening in the floor that allows a source array to be raised out of the water into the cell by an elevator. The cell that was used in these irradiations contained an array of 40 source pins arranged in a straight line. The array contained approximately 225 kCi of ^{60}Co. Our test ASICs were held inside stainless steel thermos bottles (see Figure 1) positioned approximately 2 inches from the face of the source array[3]. Cooling was provided by vortex tube coolers [7] mounted in holes drilled through the plastic thermos bottle lids.

The dose rate was 1425 rad/second as measured by an ion chamber placed inside one of the thermos bottles[4]. The uniformity of the radiation field was checked by irradiating thermoluminescent dosimeters taped to each of the chip carriers on the irradiation PCBs. The nonuniformity in the dose rate at the position of the various chip carriers was measured to be less than 6% RMS. This measurement also provided a double check of the dose rate measured with the ion chamber.

The uncollimated nature of the radiation field meant that the radiation tolerance of all components left in the cell during irradiation needed to be considered. The energy deposited by gamma rays in the steel source pins and in the air caused the air temperature in the cell to increase to $\sim$35°C during long irradiations. Gamma ray interactions in the walls of the thermos bottles directly heated the inside of the thermos bottle. In order to maintain the temperature of the test devices less than -20°C, it was necessary to precool the compressed air input to the vortex tubes and to insulate the copper tubes carrying air to the vortex tubes. Figure 3 shows the temperature of the two thermos bottles during irradiation. The precooling of the compressed air was improved after the first two long irradiations.

During the irradiations, the chip carriers were mounted in sockets on irradiation PCBs. Each irradiation PCB held four chip carriers (see Figure 1), two for PMOS packages, and one each for NMOS and cold transistor packages. Transistor bias voltages were provided by Keithley 237 SMUs (located outside the shielded irradiation cell) connected to the irradiation PCBs by long triax cables. The PMOS transistors were biased in two different ways. In one package, the drains, sources, and gates were held at 1.2V and the substrate was grounded; the other package was biased with all the gates and the substrate grounded, while the drains and sources were held at 1.2V. The gates of both the core NMOS and the I/O NMOS were biased at 1.2V; all other nodes were

[3]The standard practice for ^{60}Co irradiation calls for the electrical devices being tested to be shielded with a 1.5mm of lead followed by 0.7 - 1.0 mm of aluminum[8] "in order to minimize dose enhancement effects caused by low-energy scattered radiation." Our setup did not include a lead-aluminum shielding structure.

[4]All dosimetry was provided by Sandia National Laboratory.

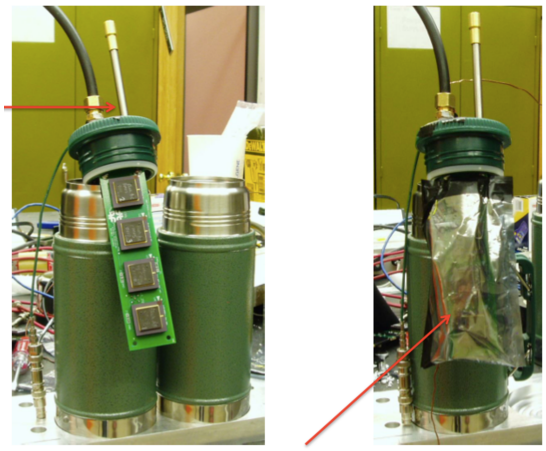

Figure 1: Pictures of a thermos bottle assembly, including an irradiation board with four test structures, before insertion of the irradiation board into the thermos bottle. In the left photo, the red arrow points to the vortex tube[7] on top of the thermos bottle lid. In the right photo, the red arrow points to an antistatic bag which wraps the irradiation board and (lemo) low-voltage cable before irradiation. These bags separate the boards and voltage cables from the not-very-dry thermos bottle environment, and provide protection from the metal thermos bottle wall (the test structures are as close to the inner thermos bottle wall as is safe, but not touching). During irradiation, copper pipe was used to deliver air to the vortex tubes.

grounded. Twelve irradiations were performed over 15 days, as shown in Table 2. After each irradiation step, a single characteristic curve was recorded for each transistor. The two SMUs were controlled via GPIB by the Labview program. The drain-source voltage was set to 1.2V and the drain-source current was measured as a function of gate voltage as the gate-source voltage was swept from 0 to 1.2V. It took ∼10 minutes to test the transistors in each package. The ASIC packages were kept at $-20°C$ in a freezer when not being tested or irradiated.

Pre-irradiation measurements of the transistors showed that a small number of transistors were destroyed either in fabrication or in the wire bonding process. Approximately half of the transistors that were irradiated were destroyed during the 15 days at Sandia. One group of 12 NMOS transistors was destroyed mechanically by mishandling. Most of the other transistors that failed also did so in groups, but without an obvious cause. We replaced the package containing the group of 12 NMOS transistors part way through the irradiation. The replacement package received a total dose of 877 Mrad.

After the irradiations, the devices were kept at $-20°C$ in a freezer that could be powered either by 120V or by 12V and transported to Fermilab. Once at Fermilab the transistors were removed from the freezer and kept at room temperature for one week. Multiple measurements were taken during this time. Then the transistors were held in an oven at $100°C$ for another week and a final set of measurements was made. This annealing schedule can be seen in Table 3.

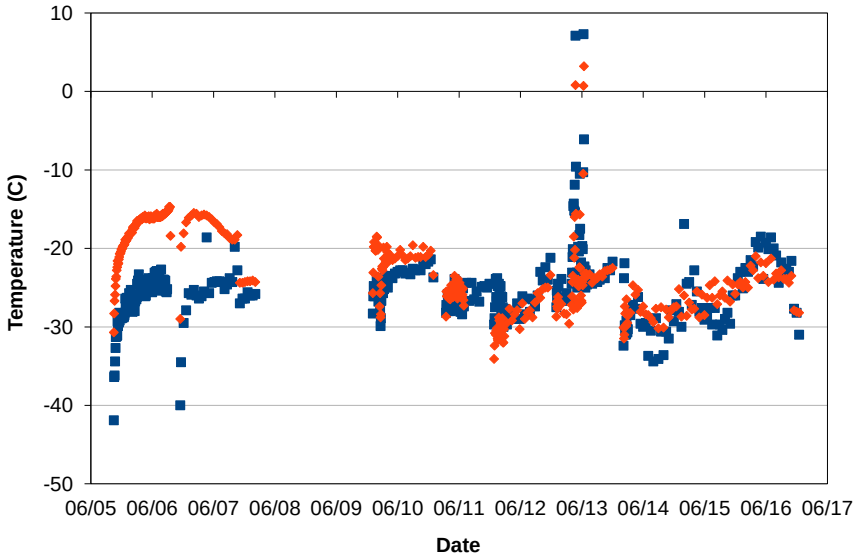

Figure 2: The temperature measured inside the two thermos bottles throughout the irradiation. The 2 day gap of no data took place over the weekend and the temperature in both thermos bottles stayed below $-20°C$ the entire time. The two spikes where the temperature reached about $8°C$ in both thermos bottles for 30 minutes occurred because the compressed air unexpectedly shut off.

Date	Length	Dose(Mrad)	Cumulative Dose(Mrad)
June 2	1 hour	5.13	5.13
June 3	1 hour	5.13	10.26
June 3	1 hour 45 mins	8.98	19.24
June 3	4 hour 15 mins	21.80	41.04
June 4-5	12 hours	61.56	102.60
June 5-6	22 hours	112.86	215.46
June 6-7	22 hours	112.86	328.32
June 9-10	22 hours	112.86	441.18
June 10-11	17 hours	87.21	528.39
June 11-12	22 hours	112.86	641.25
June 12-13	22 hours	112.86	754.11
June 13-16	66 hours	338.58	1092.69

Table 2: The irradiation schedule, showing the 2 weeks it took to get to above 1 Grad.

Annealing Schedule		
June 16-24	$-20°C$	8 Days
June 24 - July 1	Room Temperature	7 Days
July 1-8	$100°C$	7 Days

Table 3: The annealing times and temperatures of the transistors.

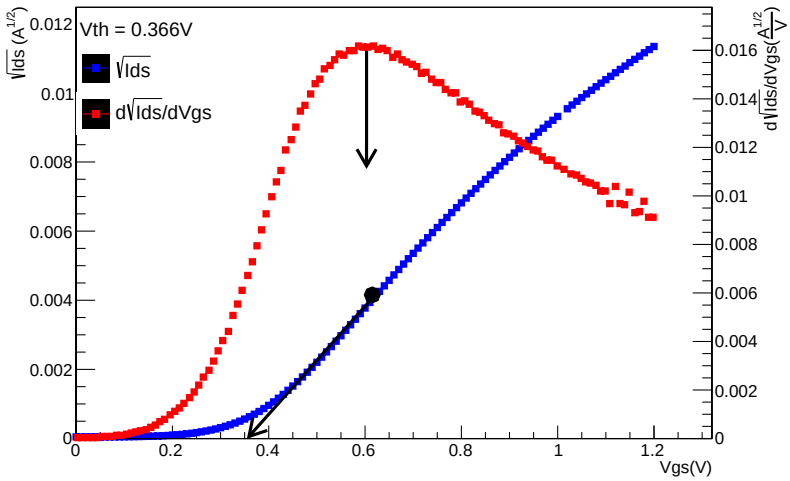

Figure 3: This figure illustrates the quadratic extrapolation method used to determine the (saturation) threshold voltage (V_{th}).

3. Analysis and Results

Two quantities were extracted from each transistor characteristic: the maximum drain-source current and the (saturation) threshold voltage (V_{th}). The quadratic extrapolation method was used to determine the threshold voltage. As shown in Figure 3, (V_{th}) is defined to be the voltage at which a line tangent to the curve $\sqrt{I_{ds}}$ vs V_{gs} at the point of maximum $\frac{d\sqrt{I_{ds}}}{dV_{gs}}$ intercepts the $I_{ds} = 0$ axis.

Figure 4 illustrates the radiation effects observed in our data. The most prominent effect is a decrease of the maximum drain-source current of core PMOS transistors. The fractional decrease is largest for the smallest PMOS transistors; the maximum drain-source current of the smallest PMOS decreased by more than a factor of two. The maximum drain-source current of core NMOS transistors also decreased, but only by $\sim 5-10\%$. No significant threshold shift was observed for any of the core transistors, but the threshold voltage of NMOS I/O transistors increased by 100 - 200 mV.

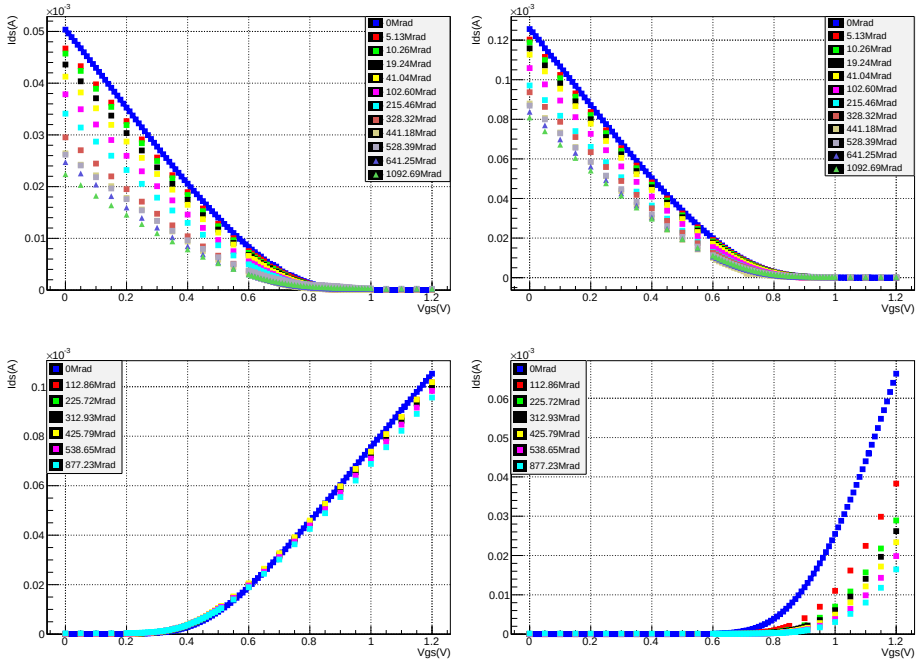

Figure 4: Transistor characteristic curves for total dose up to 1.1 Grad of a) a 120/60 core PMOS, b) a 360/60 core PMOS, and for total dose up to 877 Mrad of c) a 240/60 core NMOS, and d) a 1000/280 2.5V NMOS.

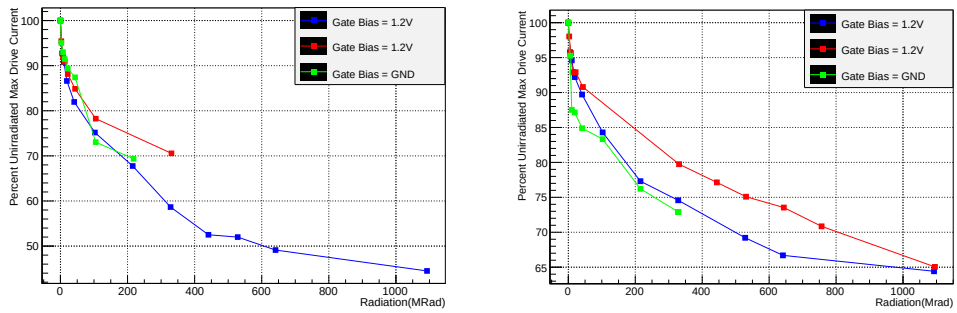

Figure 5: The change in maximum drain-source current for similar PMOS core transistors irradiated with different gate bias voltages. The graph on left is for 120/60 transistors and the graph on the right is for 360/60 transistors.

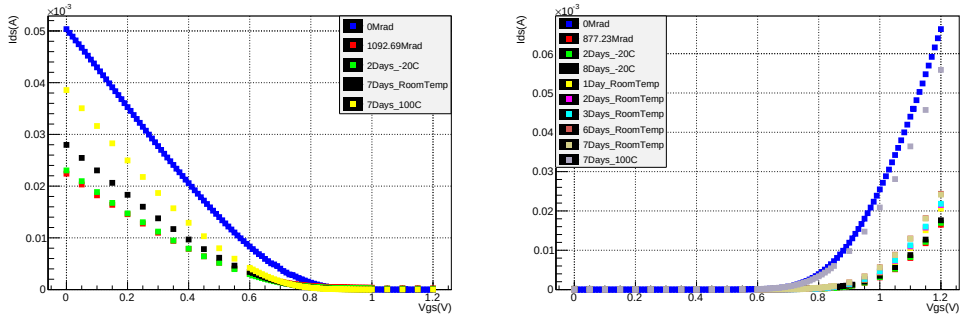

Figure 6: Transistor chararcteristic curves during the annealing period for a) a 120/60 core PMOS and b) a 1000/280 2.5V NMOS.

No significant difference was observed between the radiation-induced changes of PMOS transistors biased during the irradiation with the gate in the ON state and PMOS transistors biased with the gate in the OFF state. This is illustrated in Figure 5. We also did not observe any significant differences in the effect of radiation on the various different types of NMOS transistors tested (normal layout, enclosed layout, triple well, and zero V_{th}).

Figure 6 demonstrates the annealing effects observed in our data. Both the PMOS core transistors and the NMOS I/O transistors recovered significantly during the annealing period.

Figures 7 and 8 show the evolution of the maximum drain-source current for a representative selection of PMOS and NMOS core transistors during irradiation and annealing. A small number of measurements that we believe to be faulty were excluded from these plots. In these measurements the percent change in the current at the point of maximum transconductance from one irradiation step to the next was anomalously large (more than -18.4% or $+14\%$). Figure

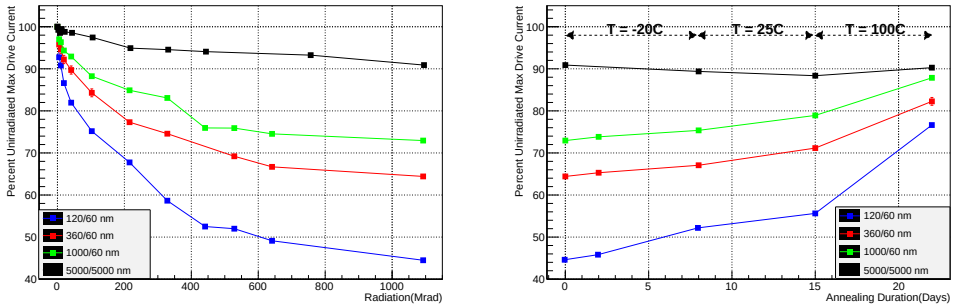

Figure 7: The graph on the left shows the loss of maximum drain-source current during irradiation for 4 PMOS core transistors. The graph on the right shows the recovery of maximum drain-source current for the same 4 transistors during and after annealing.

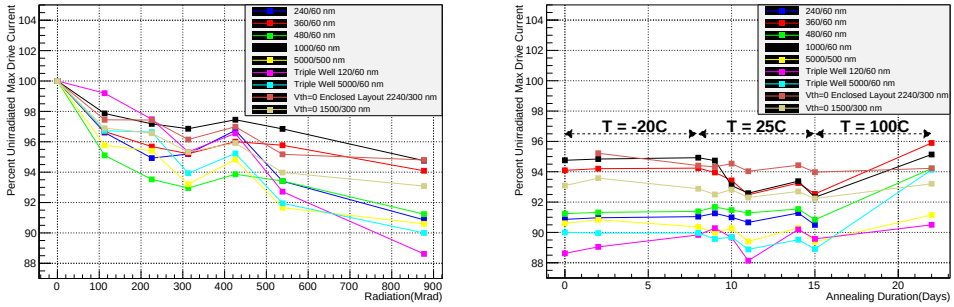

Figure 8: The graph on the left shows the loss in maximum drain-source current after each irradiation step for 9 NMOS core transistors. The graph on the right shows the change in maximum drain-source current for the same 9 transistors during and after annealing.

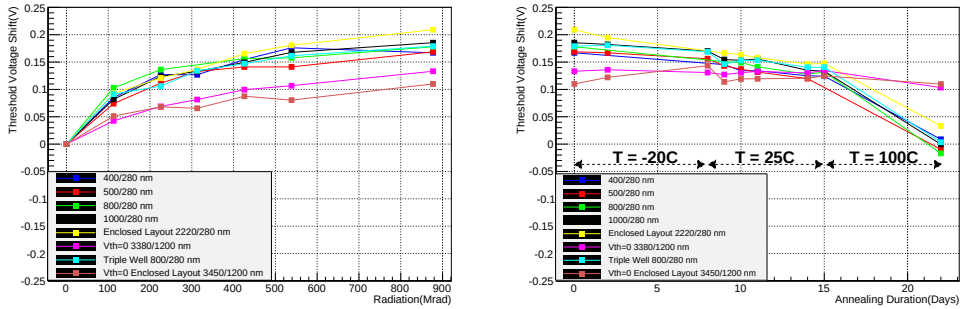

Figure 9: The shift in threshold voltage for 8 NMOS I/O transistors irradiated to 877 MRad is shown in the graph on the left, while the graph on the right shows V_T for the same 8 transistors during and after annealing. No significant annealing was observed for the two zero V_{Th} I/O transistors.

9 shows the threshold shift of NMOS I/O transistors during irradiation and annealing.

4. Summary

Previous measurements have established 65nm CMOS as the leading candidate technology for HL-LHC electronics. After an exposure of 200 Mrad, Bonacini, *et al.* reported [1], with one exception, only minor changes in transistor parameters. The exception was a significant loss of maximum drain-source current by narrow PMOS core transistors. They reported a 50% reduction in maximum drive current for a 120/60 PMOS core transistor and a 35% loss for a 360/60 PMOS core transistor. This irradiation of "cold" 65nm CMOS transistors was motivated by a concern that damage to pixel vertex detector readout electronics operated at $-20\,^{\circ}$C might be greater than observed in room temperature irradiations. Our measurements show the same pattern of effects as observed previously, but the damage is less severe than was observed at room temperature, rather than more severe.

5. Acknowledgments

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