

# Radiation Tolerance of 65nm CMOS Transistors

M. Krohn, B. Bentele, J. P. Cumalat, S. R. Wagner

*Department of Physics, University of Colorado, Boulder, Colorado 80309-0390, U.S.A.*

D. C. Christian, G. Deptuch, F. Fahim, J. Hoff, A. Shenai

*Fermi National Accelerator Laboratory, Batavia, IL 60510, U.S.A.*

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## Abstract

We report on the effects of ionizing radiation on 65nm CMOS transistors held at approximately  $-20^{\circ}\text{C}$  during irradiation. The pattern of damage observed after a total dose of 1 Grad is similar to damage reported in room temperature exposures, but we observe less damage than was observed at room temperature.

*Keywords:*

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## 1. Introduction

The need for extremely radiation tolerant electronics is one of the major issues confronting high energy physics in the era of High Luminosity running at the CERN Large Hadron Collider (HL-LHC). Tests at CERN [1], published in 2012, established 65nm CMOS as the leading candidate technology for HL-LHC electronics. Using an X-ray beam, Bonacini, *et al.* exposed 65nm transistors to a total dose of 200 Mrad. Their results showed, with one exception, relatively small changes in transistor parameters for normal layout standard gate oxide thickness (core) transistors. The exception was a dramatic loss of maximum drain-source current in the narrowest PMOS transistors. The CERN group concluded that 65nm CMOS technology can be used for HL-LHC applications with no special design considerations, except that all core devices should have width greater than 360nm.

The RD53 collaboration was formed in 2014 to further explore the feasibility of using 65nm CMOS technology to design a pixel readout chip for use at the HL-LHC [2]. The group established a total ionizing dose tolerance goal of 1 Grad. The measurements reported in this paper were done in the context of RD53. Discussions late in 2013 within RD53 centered on the fact that the data presented in reference [1], and also subsequent data collected by the CERN group and by a group from CPPM [3], contain evidence of significant room temperature annealing during the time between X-ray exposures. Both CMS and ATLAS currently plan to operate their HL-LHC pixel vertex detectors at

31 approximately  $-20^{\circ}\text{C}$ . This is because the silicon strip trackers will operate  
32 at  $-20^{\circ}\text{C}$  in order to limit leakage current in the silicon sensors, which would  
33 otherwise require much more cooling and therefore more mass in the tracking  
34 volume. Concern was expressed that 65nm circuits might experience greater  
35 radiation damage than had been observed in room temperature exposures if  
36 they were maintained at  $-20^{\circ}\text{C}$  during irradiation.

37 We report the results of an irradiation of 65nm transistors performed using  
38 the Gamma Irradiation Facility at Sandia National Laboratory [4]. The devices  
39 under test were maintained at a temperature  $\lesssim -20^{\circ}\text{C}$  during irradiation.

## 40 2. Apparatus and Technique

### 41 2.1. Test ASIC

42 A 65nm CMOS Application Specific Integrated Circuit (ASIC) containing  
43 individual transistors connected to wire bond pads was designed at Fermilab and  
44 fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC)<sup>1</sup>.  
45 The test ASIC was part of a multi project wafer submitted to TSMC through  
46 the Metal Oxide Semiconductor Implementation Service (MOSIS)<sup>2</sup>. The chip  
47 was divided into two parts, one part intended primarily for lifetime studies  
48 of devices operated at liquid argon temperature, and one part intended for  
49 radiation tolerance testing. Table 1 lists the transistors that were tested in this  
50 study. Most of the core transistor varieties available in the TSMC 65nm CMOS  
51 process are represented. As indicated in the table, there are five groups of similar  
52 transistors. Within a group, all transistors share a diode-protected gate pad,  
53 and an (unprotected) source pad. The drain of every transistor is connected to  
54 its own wire bonding pad. We tested PMOS and NMOS core (1.2V) transistors,  
55 and NMOS I/O (2.5V) transistors (with double thickness gate oxide).

### 56 2.2. ASIC package, test equipment, and measurement procedures

57 The test ASICs were wire bonded into pin grid array chip carriers so that  
58 they could be irradiated on simple printed circuit boards (PCBs) containing no  
59 active components other than the test ASICs, and tested on more complicated  
60 PCBs. Transistor characteristics were measured with the chip carriers mounted  
61 on boards containing switches that allowed individual transistors to be measured  
62 one at a time. The number of pads on the test ASICs was too large to allow all  
63 pads to be wire bonded in one package, given the chosen chip carrier, so three  
64 different packages with different wire bonding patterns were made. One package  
65 had bonds only to devices intended for cold tests. NMOS transistors were  
66 wire bonded in the second package, and PMOS transistors were wire bonded in  
67 the third package. The devices intended for cold tests are all large transistors

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<sup>1</sup>Our test chip was fabricated at TSMC fab 14. The devices tested earlier at CERN were fabricated at TSMC fab 12 [5].

<sup>2</sup>MOSIS is operated by the Information Sciences Institute at the University of Southern California.

Standard Gate 1	PMOS	120/60, 360/60, 600/60, 1000/60
Standard Gate 2	PMOS	5000/500, 5000/5000
Standard Gate 1	NMOS	120/60, 240/60, 360/60, 480/60, 600/60, 1000/60
Standard Gate 2	NMOS	5000/500, 5000/5000, ELT 2050/60, $zV_{th}$ 1500/300, $zV_{th}$ ELT 2240/300, TW 120/60, TW 5000/60
Double Gate Oxide Thickness	NMOS	400/280, 500/280, 800/280, 1000/280, 5000/500, 5000/5000, ELT 2220/280, $zV_{th}$ 3380/1200, TW 400/280, TW 800/280, $zV_{th}$ ELT 3450/1200

Table 1: Transistors tested in this study: The numbers indicate transistor size ( $W/L =$  channel Width/Length), ELT indicates an Enclosed Layout Transistor,  $zV_{th}$  indicates a transistor with threshold voltage = 0, and TW indicates Triple Well NMOS transistors laid out with the Pwell within a deep Nwell.

68 unlikely to be used in a pixel readout ASIC. They have been excluded from this  
69 analysis.

70 A different PCB was used to test each ASIC package. These test PCBs were  
71 connected to two Keithley 237 Source Measurement Units (SMUs) using triax  
72 cables and to a National Instruments USB-6501 I/O board by a twisted-pair  
73 ribbon cable. The I/O board was connected to a USB port of a laptop computer  
74 running Labview. Bias voltage for the protection diodes was generated by a  
75 voltage regulator on the test PCB from the 5V provided by the laptop USB  
76 port. The Labview program controlled solid state switches on the test PCB  
77 that connected one of the SMUs to a single gate pad at a time; unused gates  
78 were grounded. The program controlled LEDs on the test PCB to indicate how  
79 mechanical (rotary) switches on the test PCB should be set to connect the other  
80 SMU to a single transistor drain. All three voltage sources were referenced to a  
81 common ground plane on the test PCB, and the source pads for all transistors  
82 in a package were connected directly to this ground. The fact that we did  
83 not separate the return current path for the two SMUs, together with possible  
84 parasitic circuits involving the protection diodes and the solid state switches  
85 in the OFF state, made it impossible for us to accurately measure the leakage  
86 current of transistors in the ASIC packages.

### 87 2.3. Irradiation

88 The Sandia National Laboratory Gamma Irradiation Facility (GIF) uses  
89  $^{60}\text{Co}$  sources to provide controlled doses of ionizing radiation.  $^{60}\text{Co}$  decays by  
90 beta decay to an excited state of  $^{60}\text{Ni}$ . The  $^{60}\text{Ni}$  relaxes to the ground state  
91 by emitting two gamma rays of energy 1.17 and 1.33 MeV [6]. At the Sandia  
92 GIF,  $^{60}\text{Co}$  is held in stainless steel “source pins” that are 3/8 inch diameter

93 and 18 inches long. A number of source pins are mounted in an array and to  
94 first order, none of the beta electrons escapes the steel source pins. When not  
95 in use, the sources are kept at the bottom of an 18 foot deep pool of deionized  
96 water which provides shielding. The facility has three shielded irradiation cells  
97 in a single high bay area above the shielding pool. Each irradiation cell has an  
98 opening in the floor that allows a source array to be raised out of the water into  
99 the cell by an elevator. The cell that was used in these irradiations contained  
100 an array of 40 source pins arranged in a straight line. The array contained  
101 approximately 225 kCi of  $^{60}\text{Co}$ . Our test ASICs were held inside stainless steel  
102 thermos bottles (see Figure 1) positioned approximately 2 inches from the face  
103 of the source array<sup>3</sup>. Cooling was provided by vortex tube coolers [7] mounted  
104 in holes drilled through the plastic thermos bottle lids.

105 The dose rate was 1425 rad/second as measured by an ion chamber placed  
106 inside one of the thermos bottles<sup>4</sup>. The uniformity of the radiation field was  
107 checked by irradiating thermoluminescent dosimeters taped to each of the chip  
108 carriers on the irradiation PCBs. The nonuniformity in the dose rate at the  
109 position of the various chip carriers was measured to be less than yy%. This  
110 measurement also provided a double check of the dose rate measured with the  
111 ion chamber.

112 The uncollimated nature of the radiation field meant that the radiation  
113 tolerance of all components left in the cell during irradiation needed to be con-  
114 sidered. The energy deposited by gamma rays in the steel source pins and in  
115 the air caused the air temperature in the cell to increase to  $\sim 35^\circ\text{C}$  during long  
116 irradiations. Gamma ray interactions in the walls of the thermos bottles directly  
117 heated the inside of the thermos bottle. In order to maintain the temperature  
118 of the test devices less than  $-20^\circ\text{C}$ , it was necessary to precool the compressed  
119 air input to the vortex tubes and to insulate the copper tubes carrying air to  
120 the vortex tubes. Figure 3 shows the temperature of the two thermos bottles  
121 during irradiation. The precooling of the compressed air was improved after the  
122 first two long irradiations.

123 During the irradiations, the chip carriers were mounted in sockets on ir-  
124 radiation PCBs. Each irradiation PCB held four chip carriers (see Figure 1),  
125 two for PMOS packages, and one each for NMOS and cold transistor packages.  
126 Transistor bias voltages were provided by Keithley 237 SMUs (located outside  
127 the shielded irradiation cell) connected to the irradiation PCBs by long triax  
128 cables. The PMOS transistors were biased in two different ways. In one pack-  
129 age, the drains, sources, and gates were held at 1.2V and the substrate was  
130 grounded; the other package was biased with all the gates and the substrate  
131 grounded, while the drains and sources were held at 1.2V. The gates of both  
132 the core NMOS and the I/O NMOS were biased at 1.2V; all other nodes were

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<sup>3</sup>The standard practice for  $^{60}\text{Co}$  irradiation calls for the electrical devices being tested to be shielded with a 1.5mm of lead followed by 0.7 - 1.0 mm of aluminum[8] "in order to minimize dose enhancement effects caused by low-energy scattered radiation." Our setup did not include a lead-aluminum shielding structure.

<sup>4</sup>All dosimetry was provided by Sandia National Laboratory.

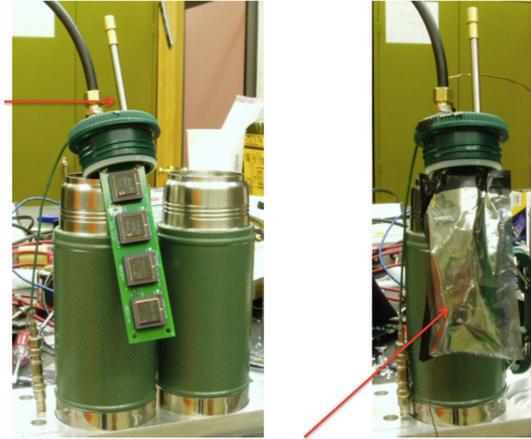


Figure 1: Pictures of a thermos bottle assembly, including an irradiation board with four test structures, before insertion of the irradiation board into the thermos bottle. In the left photo, the red arrow points to the vortex tube[7] on top of the thermos bottle lid. In the right photo, the red arrow points to an antistatic bag which wraps the irradiation board and (lemo) low-voltage cable before irradiation. These bags separate the boards and voltage cables from the not-very-dry thermos bottle environment, and provide protection from the metal thermos bottle wall (the test structures are as close to the inner thermos bottle wall as is safe, but not touching). During irradiation, copper pipe was used to deliver air to the vortex tubes.

133 grounded. Twelve irradiations were performed over 15 days, as shown in Table  
 134 2. After each irradiation step, a single characteristic curve was recorded for each  
 135 transistor. The two SMUs were controlled via GPIB by the Labview program.  
 136 The drain-source voltage was set to 1.2V and the drain-source current was measured  
 137 as a function of gate voltage as the gate-source voltage was swept from 0  
 138 to 1.2V. It took  $\sim 10$  minutes to test the transistors in each package. The ASIC  
 139 packages were kept at  $-20^{\circ}\text{C}$  in a freezer when not being tested or irradiated.

140 Pre-irradiation measurements of the transistors showed that a small number  
 141 of transistors were destroyed either in fabrication or in the wire bonding process.  
 142 Approximately half of the transistors that were irradiated were destroyed during  
 143 the irradiation. One group of 12 NMOS transistors was destroyed mechanically  
 144 by mishandling. Most of the other transistors that failed also did so in groups,  
 145 but without an obvious cause. We replaced the package containing the group  
 146 of 12 NMOS transistors part way through the irradiation. The replacement  
 147 package received a total dose of 877 Mrad.

148 After the irradiations, the devices were kept at  $-20^{\circ}\text{C}$  in a freezer that  
 149 could be powered either by 120V or by 12V and transported to Fermilab. Once  
 150 at Fermilab the transistors were removed from the freezer and kept at room  
 151 temperature for one week. Multiple measurements were taken during this time.  
 152 Then the transistors were held in an oven at  $100^{\circ}\text{C}$  for another week and a final  
 153 set of measurements was made. This annealing schedule can be seen in Table 3.

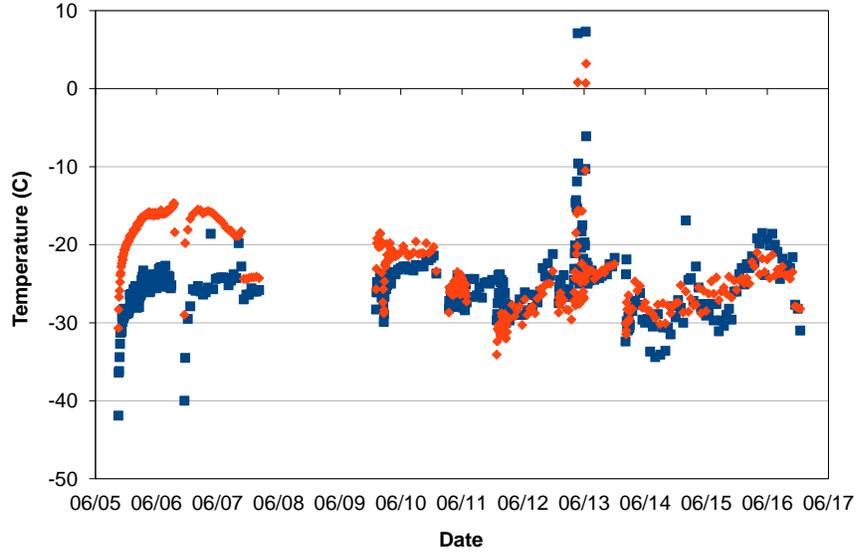


Figure 2: The temperature measured inside the two thermos bottles throughout the irradiation. The 2 day gap of no data took place over the weekend and the temperature in both thermos bottles stayed below  $-20^{\circ}\text{C}$  the entire time. The two spikes where the temperature reached about  $8^{\circ}\text{C}$  in both thermos bottles for 30 minutes because the compressed air unexpectedly shut off.

Date	Length	Dose(Mrad)	Cumulative Dose(Mrad)
June 2	1 hour	5.13	5.13
June 3	1 hour	5.13	10.26
June 3	1 hour 45 mins	8.98	19.24
June 3	4 hour 15 mins	21.80	41.04
June 4-5	12 hours	61.56	102.60
June 5-6	22 hours	112.86	215.46
June 6-7	22 hours	112.86	328.32
June 9-10	22 hours	112.86	441.18
June 10-11	17 hours	87.21	528.39
June 11-12	22 hours	112.86	641.25
June 12-13	22 hours	112.86	754.11
June 13-16	66 hours	338.58	1092.69

Table 2: The irradiation schedule, showing the 2 weeks it took to get to above 1 Grad.

Annealing Schedule		
June 16-24	$-20^{\circ}C$	8 Days
June 24 - July 1	Room Temperature	7 Days
July 1-8	$100^{\circ}C$	7 Days

Table 3: The annealing times and temperatures of the transistors.

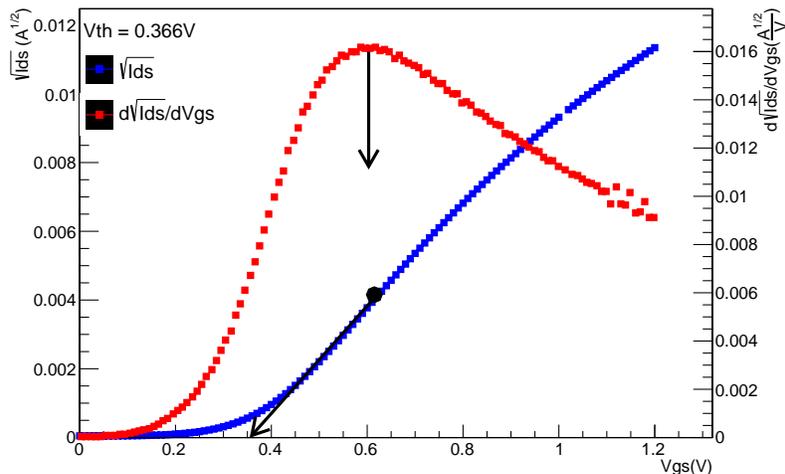


Figure 3: This figure illustrates the quadratic extrapolation method used to determine the (saturation) threshold voltage ( $V_{th}$ ).

### 154 3. Analysis and Results

155 Two quantities were extracted from each transistor characteristic: the maximum  
 156 drain-source current and the (saturation) threshold voltage ( $V_{th}$ ). The  
 157 quadratic extrapolation method was used to determine the threshold voltage.  
 158 As shown in Figure 3, ( $V_{th}$ ) is defined to be the voltage at which a line tangent  
 159 to the curve  $\sqrt{I_{ds}}$  vs  $V_{gs}$  at the point of maximum  $\frac{d\sqrt{I_{ds}}}{dV_{gs}}$  intercepts the  $I_{ds} = 0$   
 160 axis.

161 Figure 4 illustrates the radiation effects observed in our data. The most  
 162 prominent effect is a decrease of the maximum drain-source current of core  
 163 PMOS transistors. The fractional decrease is largest for the smallest PMOS  
 164 transistors; the maximum drain-source current of the smallest PMOS decreased  
 165 by more than a factor of two. The maximum drain-source current of core NMOS  
 166 transistors also decreased, but only by  $\sim 5 - 10\%$ . No significant threshold shift  
 167 was observed for any of the core transistors, but the threshold voltage of NMOS  
 168 I/O transistors increased by 100 - 200 mV.

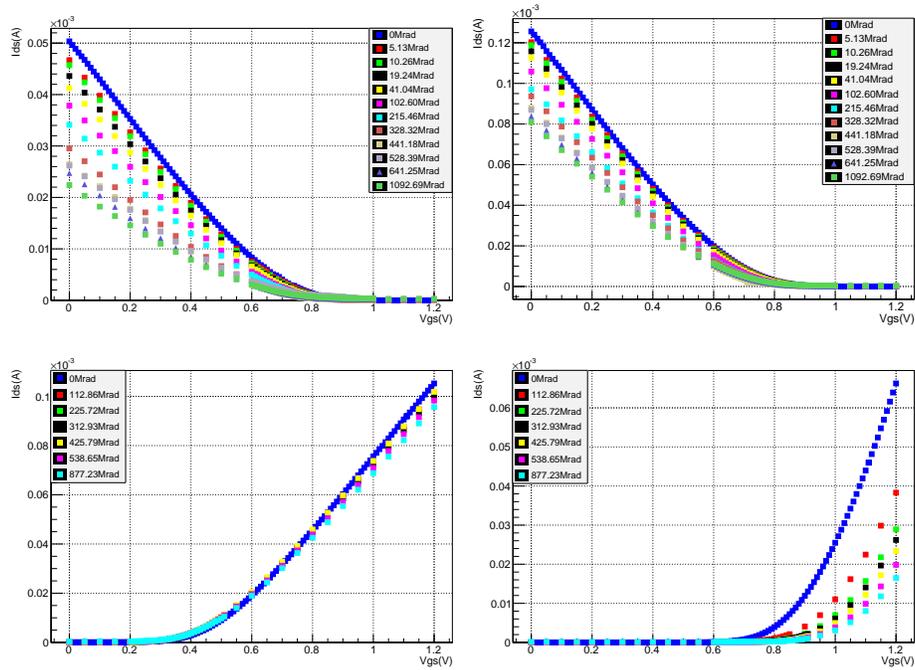


Figure 4: Transistor characteristic curves for total dose up to 1.1 Grad of a) a 120/60 core PMOS, b) a 360/60 core PMOS, and for total dose up to 877 Mrad of c) a 240/60 core NMOS, and d) a 1000/280 2.5V NMOS.

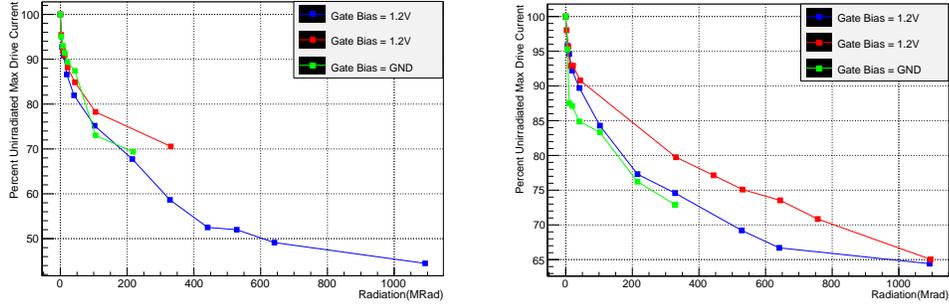


Figure 5: The change in maximum drain-source current for similar PMOS core transistors irradiated with different gate bias voltages. The graph on the left is for 120/60 transistors and the graph on the right is for 360/60 transistors.

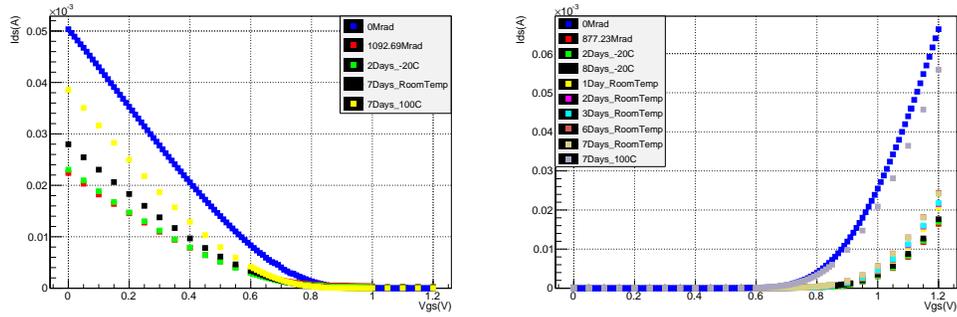


Figure 6: Transistor characteristic curves during the annealing period for a) a 120/60 core PMOS and b) a 1000/280 2.5V NMOS.

169 No significant difference was observed between the radiation-induced changes  
 170 of PMOS transistors biased during the irradiation with the gate in the ON state  
 171 and PMOS transistors biased with the gate in the OFF state. This is illustrated  
 172 in Figure 5. We also did not observe any significant differences in the effect of  
 173 radiation on the various different types of NMOS transistors tested (normal  
 174 layout, enclosed layout, triple well, and zero  $V_{th}$ ).

175 Figure 6 demonstrates the annealing effects observed in our data. Both the  
 176 PMOS core transistors and the NMOS I/O transistors recovered significantly  
 177 during the annealing period.

178 Figures 7 and 8 show the evolution of the maximum drain-source current for a  
 179 representative selection of PMOS and NMOS core transistors during irradiation  
 180 and annealing. A small number of measurements that we believe to be faulty  
 181 were excluded from these plots. In these measurements the percent change in  
 182 the current at the point of maximum transconductance from one irradiation  
 183 step to the next was anomalously large (more than  $-18.4\%$  or  $+14\%$ ). Figure

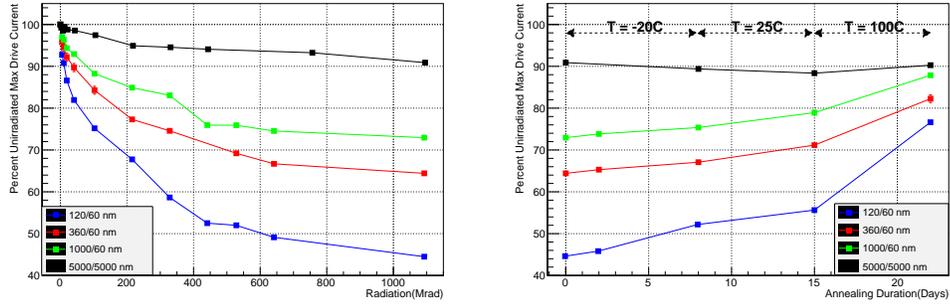


Figure 7: The graph on the left shows the loss of maximum drain-source current during irradiation for 4 PMOS core transistors. The graph on the right shows the recovery of maximum drain-source current for the same 4 transistors during and after annealing.

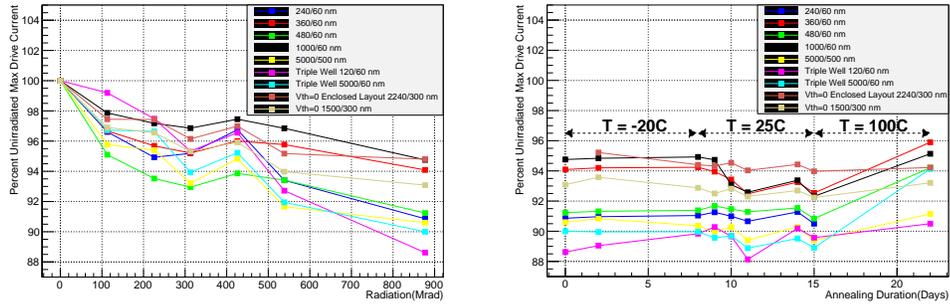


Figure 8: The graph on the left shows the loss in maximum drain-source current after each irradiation step for 9 NMOS core transistors. The graph on the right shows the change in maximum drain-source current for the same 9 transistors during and after annealing.

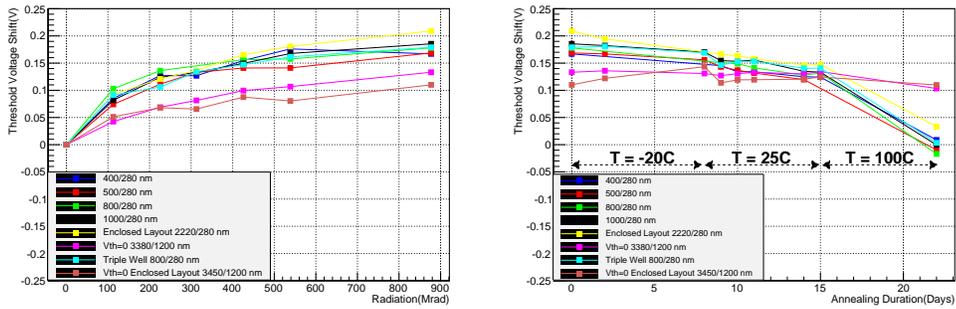


Figure 9: The shift in threshold voltage for 8 NMOS I/O transistors irradiated to 877 Mrad is shown in the graph on the left, while the graph on the right shows  $V_T$  for the same 8 transistors during and after annealing. No significant annealing was observed for the two zero  $V_{Th}$  I/O transistors.

184 9 shows the threshold shift of NMOS I/O transistors during irradiation and  
185 annealing.

#### 186 4. Summary

187 Previous measurements have established 65nm CMOS as the leading candi-  
188 date technology for HL-LHC electronics. After an exposure of 200 Mrad,  
189 Bonacini, *et al.* reported [1], with one exception, only minor changes in transis-  
190 tor parameters. The exception was a significant loss of maximum drain-source  
191 current by narrow PMOS core transistors. They reported a 50% reduction in  
192 maximum drive current for a 120/60 PMOS core transistor and a 35% loss for a  
193 360/60 PMOS core transistor. This irradiation of “cold” 65nm CMOS transis-  
194 tors was motivated by a concern that damage to pixel vertex detector readout  
195 electronics operated at  $-20^{\circ}\text{C}$  might be greater than observed in room tem-  
196 perature irradiations. Our measurements show the same pattern of effects as  
197 observed previously, but the damage is less severe than was observed at room  
198 temperature, rather than more severe.

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