Hardening ASICs against radiation effects

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Outline

✓ Summary of radiation effects
  • Total Ionizing Dose (TID)
  • Single Event Effects (SEE)

✓ Hardness By Design (HBD) techniques
  • Foreword
  • TID: Total Ionizing Dose
    • TID and scaling
    • Solutions
  • SEE: Single Event Effects
    • SEEs and scaling
    • Solutions
  • Summary & Conclusion
Summary of radiation effects

Cumulative effects

Total Ionizing Dose (TID)
- Potentially all components

Displacement damage
- Bipolar technologies
- Optocouplers
- Optical sources
- Optical detectors (photodiodes)

Single Event Effects (SEE)

Permanent SEEs
- SEL
- CMOS technologies
- SEB
- Power MOSFETs, BJT and diodes
- SEGR
- Power MOSFETs

Transient SEEs
- Combinational logic
- Operational amplifiers

Static SEEs
- SEU, SEFI
- Digital ICs
TID in MOS structures

1. Poly
2. SiO₂
3. Si

+ V -
+ V -
+ V -
+ V -

Trapped charge ALWAYS POSITIVE!

Interface states Can trap both e⁻ and h⁺

ALWAYS POSITIVE!
Contributions to the $V_T$ shift

- Oxide charges
- Interface states

N-channel
- Before irradiation
  - $I_1$
  - $I_2$

P-channel
- Before irradiation
  - $I_1$

Before irradiation

$V_{GS}$ $V_T1$ $V_T2$ $V_T$
Transistor level leakage

Parasitic MOS

Parasitic channel

Trapped positive charge

Field oxide

Bird’s beak

Source

Drain
Transistor level leakage

This is for LOCOS, very similar for STI

log $I_D$

$V_{GS}$

GATE

“CENTRAL” (main) MOS TRANSISTOR

BIRD’S BEAKS

This is for LOCOS, very similar for STI

GATE

“CENTRAL” (main) MOS TRANSISTOR

BIRD’S BEAKS

log $I_D$

$V_{GS}$
Transistor level leakage: example

NMOS - 0.7 μm technology - $t_{ox} = 17$ nm

Threshold voltage shift
IC level leakage

The charges trapped in the thick oxide (LOCOS or STI) decrease the Vth of the MOS structure, and the p substrate can be inverted even in the absence of an electric field. A leakage current can appear.
TID-induced failure

✓ In modern technologies, leakage current is typically the killer
TID in CMOS

Summary of the problems

✓ Main transistor:
  - Threshold voltage shift, transconductance and noise degradation
  - Effects get negligible in modern deep submicron (as from 250-180 nm techs)

✓ Parasitic leakage paths:
  - Source – drain leakage
  - Leakage between devices
  - This are still potentially deleterious – although things looks to be better as from 130nm techs
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Ionization from different radiation

- Traceable to the energy deposition initiated by one single particle, in a precise instant in time. Due to its stochastic nature, this can happen at any time – even at the very beginning of the irradiation.
- Which particles can induce SEEs? In the figure below, a schematic view of the density of e-h pairs created by different radiation is shown.

[Diagram showing photon (X, γ), heavy ion, proton, and neutron interactions with silicon, illustrating different densities of e-h pairs.]
Density of e-h pairs is important (1)

- Not all the free charge (e-h pairs) generated by radiation contributes to SEEs. Only charge in a given volume, where it can be collected in the relevant amount of time by the appropriate circuit node, matters.

1. Ion strike: ionization takes place along the track (column of high-density pairs)

2. Charges start to migrate in the electric field across the junctions. Some drift (fast collection, relevant for SEEs), some diffuse (slow collection, less relevant for SEEs)

3. Charges are collected at circuit nodes. Note that, if the relevant node for the SEE is the p+ diffusion, not all charge deposited by the ion is collected there.
Density of e-h pairs is important (2)

Of all e-h pairs created by radiation, only those in (roughly) this volume are collected fast enough to contribute to an SEE at the node corresponding to the p+ diffusion (for instance, S or D of a PMOS FET). Density of pairs in this region determines if the SEE takes place or not! This is called the “SENSITIVE VOLUME” (SV).

The density of pairs depends on the stopping power of the particle, or $dE/dx$, or Linear Energy Transfer (LET). The figure above (right) shows this quantity in Si for different particles. Even protons, at their maximum stopping power, can not induce SEE in electronics circuits. Only ions, either directly from the radiation environment or from nuclear interaction of radiation ($p$, $n$, ...) in Silicon can deposit enough energy in the SV to induce SEEs.

Warning: data points are approximate in this figure.
Single Event Upset (SEU) (1)

The e-h pairs created by an ionizing particle can be collected by a junction that is part of a circuit where a logic level is stored (logic 0 or 1). This can induce the “flip” of the logic level stored. This event is called an “upset” or a “soft error”.

This typically happens in memories and registers. The following example is for an SRAM cell.

![Diagram of SRAM cell with e-h pairs, junction, and logic levels](image_url)
Single Event Upset (SEU) (2)

1. Initial condition
(correct value stored)

Charge collected at the drain of NMOS T1 tends to lower the potential of the node B to gnd. PMOS T2 provides current from Vdd to compensate, but has a limited current capability. If the collected charge is large enough, the voltage of node B drops below Vdd/2.

2. Final condition
(wrong value stored)

When node B drops below Vdd/2, the other inverter in the SRAM cell changes its output (node A) to logic 1. This opens T2 and closes T1, latching the wrong data in the memory cell.
“Digital” Single Event Transient (SET)

- Particle hit in combinatorial logic: with modern fast technologies, the induced pulse can propagate through the logic until it is possibly latched in a register.
- Latching probability proportional to clock frequency.
- Linear behaviour with clock frequency is observed.

\[
\text{Total Error} = \text{SET} + \text{SEU}
\]
Single Event Latchup (SEL)

Electrical latchup might be initiated by electrical transients on input/output lines, elevated T or improper sequencing of power supply biases. These modes are normally addressed by the manufacturer.

Latchup can be initiated by ionizing particles (SEL) in any place of the circuit (not only IOs)

A.H. Johnston et al., IEEE TNS, Apr. 1996
# Particles and damages

<table>
<thead>
<tr>
<th>Radiation</th>
<th>TID</th>
<th>Displacement (NIEL)</th>
<th>SEE</th>
</tr>
</thead>
<tbody>
<tr>
<td>X-rays $^{60}$Co $\gamma$</td>
<td>Expressed in SiO$_2$ Almost identical in Si or SiO$_2$</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>p</td>
<td>Equivalences in Si$^5$ @60MeV $10^{11}$p/cm$^2$=13.8krd @100MeV $10^{11}$p/cm$^2$=9.4krd @150MeV $10^{11}$p/cm$^2$=7.0krd @200MeV $10^{11}$p/cm$^2$=5.8krd @250MeV $10^{11}$p/cm$^2$=5.1krd @300MeV $10^{11}$p/cm$^2$=4.6krd @23GeV $10^{11}$p/cm$^2$=3.2krd</td>
<td>Equivalences in Si$^5$* @53MeV 1 p/cm$^2$ = 1.25 n/cm$^2$ @98MeV 1 p/cm$^2$ = 0.92 n/cm$^2$ @154MeV 1 p/cm$^2$ = 0.74 n/cm$^2$ @197MeV 1 p/cm$^2$ = 0.66 n/cm$^2$ @244MeV 1 p/cm$^2$ = 0.63 n/cm$^2$ @294MeV 1 p/cm$^2$ = 0.61 n/cm$^2$ @23GeV 1 p/cm$^2$ = 0.50 n/cm$^2$</td>
<td>Only via nuclear interaction. Max LET of recoil in Silicon = 15MeVcm$^2$mg$^{-1}$</td>
</tr>
<tr>
<td>n</td>
<td>Negligible</td>
<td>Equivalences in Si$^5$* @1MeV 1 n/cm$^2$ = 0.81 n/cm$^2$ @2MeV 1 n/cm$^2$ = 0.74 n/cm$^2$ @14MeV 1 n/cm$^2$ = 1.50 n/cm$^2$</td>
<td>As for protons, actually above 20MeV p and n can roughly be considered to have the same effect for SEEs</td>
</tr>
<tr>
<td>Heavy Ions</td>
<td>Negligible for practical purposes (example: $10^6$ HI with LET=50MeVcm$^2$mg$^{-1}$ deposit about 800 rd)</td>
<td>Negligible</td>
<td>Yes</td>
</tr>
</tbody>
</table>

$^5$ Energy here is only kinetic (for total particle energy, add the rest energy mc$^2$)

*The equivalence is referred to “equivalent 1Mev neutrons”, where the NIEL of “1Mev neutrons” is DEFINED to be 95 MeVmb. This explains why for 1MeV neutrons the equivalence is different than 1
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Foreword

✓ What we will be talking about:
  • ASICs (application-specific ICs)
  • CMOS technologies only
  • Effects: TID, SEU, SEL

  • How to conceive ASICs reliably able of surviving to and functioning in a radiation environment
Radiation effects and $t_{ox}$ scaling

Damage decreases with gate oxide thickness

Gate oxides in commercial CMOS technologies did follow the curve drawn by Saks and co-workers!
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Radiation hard CMOS processes

- “Direct solution”: technology hardening
- TID hardness is guaranteed

but

- Low volume in fabs => yield can be low, and unreliable radiation performance for large quantities
- Cost is very high
- Very limited number of processes still available today, and risk of unavailability in the long run
- Analog performance often not very well characterized
Radiation-tolerant layout (ELT)
The heavily doped p+ guardring "interrupts" possible conductive paths (inverted p substrate), hence preventing inter-device leakage currents.
Radiation tolerant approach

\[ \Delta V_{th} \propto t_{ox}^{n} + \text{ELT's and guard rings} = \text{TID Radiation Tolerance} \]
Effectiveness of ELTs

0.7 μm technology - W/L = 2000/1.5

![Graph showing the effectiveness of ELTs with different currents and voltages. The graph includes three lines: Prerad, After 1 Mrad, and After 1 Mrad (ELT). The x-axis represents the voltage (V) ranging from -1 to 3.5, and the y-axis represents the current (A) ranging from 1.E-13 to 1.E-02.](image-url)
Effectiveness of ELTs

0.25 μm technology - W/L = 30/0.4 - ELT

Prerad and after 13 Mrad
Field oxide leakage

FOXFET 14.4/2.6 without gate, with guardring
0.5 μm technology

VD [V]

I_d [A]

1.E-12
1.E-11
1.E-10

anneal

1.9 Mrad

420 Krad

Prerad

TWEPP 2007, Prague
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Advantages of this approach

✓ Relies on physics (thickness of gate oxide): not process-dependent
✓ Allows for using state-of-the-art technologies:
  • Low power
  • High performance
  • High throughput, high yield, short turnaround times
  • Low cost
Difficulties for this approach

- Peculiar ELT behaviour
  - Modeling of ELT (size W/L?)
  - Limitation in aspect ratio
  - Asymmetry
- Lack of commercial library for digital design
- Loss of density
- Yield and reliability???
Modeling of ELTs (1)
Modeling of ELTs (2)

\[ \left( \frac{W}{L} \right)_{\text{eff}} = 4 \frac{2 \alpha}{\ln \frac{d'}{d'} - 2 \alpha L_{\text{eff}}} + 2K \frac{1 - \alpha}{1.13 \cdot \ln \frac{1}{\alpha}} + 3 \frac{d - d'}{L_{\text{eff}}} \]

<table>
<thead>
<tr>
<th>L_{\text{drawn}}</th>
<th>Estimated (W/L)_{\text{eff}}</th>
<th>Extracted (W/L)_{\text{eff}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.28</td>
<td>14.8</td>
<td>15</td>
</tr>
<tr>
<td>0.36</td>
<td>11.3</td>
<td>11.2</td>
</tr>
<tr>
<td>0.5</td>
<td>8.3</td>
<td>8.3</td>
</tr>
<tr>
<td>1</td>
<td>5.1</td>
<td>5.2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>3.2</td>
</tr>
<tr>
<td>5</td>
<td>2.6</td>
<td>2.6</td>
</tr>
</tbody>
</table>

- 1 shape only supported (size of “c” fixed)
- Custom routines and layers integrated in design kit for extraction/design checking/computation
Limitation in the aspect ratio

Aspect ratio = W/L

Gate Length [μm]

Effective aspect ratio

0  1  2  3  4  5  6  7  8  9  10

2  3  4  5  6  7  8  9  10  11  12  13  14  15
Asymmetry (1)

\[ L = 0.28 \, \mu m \quad G_{Di} = 11.9 \, \mu S \quad G_{DO} = 9.6 \, \mu S \]

\[ I_{\text{drain}} \quad V_{ds} \quad [A] \quad [V] \]

- Drain Inside
- Drain Outside
Asymmetry (2)

![Graph showing output cond. vs gate length for different gate lengths and transistor types.]

Table:

<table>
<thead>
<tr>
<th>L (μm)</th>
<th>ΔG/G_{DI}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.28</td>
<td>19 %</td>
</tr>
<tr>
<td>0.36</td>
<td>23 %</td>
</tr>
<tr>
<td>0.5</td>
<td>33 %</td>
</tr>
<tr>
<td>1</td>
<td>53 %</td>
</tr>
<tr>
<td>3</td>
<td>70 %</td>
</tr>
<tr>
<td>5</td>
<td>75 %</td>
</tr>
</tbody>
</table>
Lack of commercial library (1)

Radiation tolerant design:
- Use of enclosed NMOS transistors
- Use of guard rings to isolate all $n^+$ diffusions at different potentials (including $n$-wells)

NAND3
Lack of commercial library (2)

✓ Example of core cells
Lack of commercial library (3)

List of Library Standard Cells

TWEPP 2007, Prague

Federico Faccio – CERN/PH
Existing libraries

✓ List is not exclusive:
  - CERN in 0.25\(\mu m\)
    - “Daughter” libraries in PSI, LBL, Fermilab
  - IMEC (for ESA) in 0.18\(\mu m\)
  - Mission Research Corporation (for Aerospace Corporation) in 0.18\(\mu m\)
Loss of density

- Radiation Tolerant techniques introduce a ~70% layout area overhead

- Gate density is 8 times larger when compared to a 0.8μm technology
  - Example: ring oscillator with 1280 inverters in 0.8 and 0.25mm technologies (0.25 uses the CERN radtol library)

<table>
<thead>
<tr>
<th></th>
<th>Standard</th>
<th>Rad-Tol</th>
<th>Penalty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter</td>
<td>33.6 μm²</td>
<td>50.9 μm²</td>
<td>34 %</td>
</tr>
<tr>
<td>2-in NAND</td>
<td>46.0 μm²</td>
<td>119.0 μm²</td>
<td>61 %</td>
</tr>
<tr>
<td>2-in NOR</td>
<td>47.8 μm²</td>
<td>80.0 μm²</td>
<td>41 %</td>
</tr>
<tr>
<td>Static D-F/F</td>
<td>153.0 μm²</td>
<td>533.1 μm²</td>
<td>71 %</td>
</tr>
<tr>
<td>Static D-F/F SR</td>
<td>188.1 μm²</td>
<td>572.0 μm²</td>
<td>75 %</td>
</tr>
</tbody>
</table>

Area: a) 650,400 μm²  b) 82,350 μm²
Yield and reliability?

- Construction analysis performed on several chips
- Circuits produced, qualified and tested in thousands (100 different designs!)
- No concern on yield or reliability found yet…
“Large” scale production

- Relatively large number of projects in production, for quantities up to almost 600 wafers (200mm size). Total production in excess of 3000 wafers.

Production summary

- Volume per project
- N of wafers produced
- N of projects in production

Years: 1999 to 2006
ASICs examples

- APV25: readout of Silicon tracker detector of the CMS experiment
  - 128 channels, analog output

- Alice Pixel1, readout of silicon pixel detector of the ALICE experiment
  - 2.1cm², 8000 analog channels, 13M transistors

- GOL, optical link driver (serializer + laser driver) @ 1.6 Gbit/s

- CCU, control chip for the CMS tracker detector
  - (fully digital chip, 120kgates)
Other edgeless designs

✓ Other “edgeless” transistor designs are possible, but not all yield radiation tolerance in 130nm or below

Ringed Source

Butterfly

Ringed Interdigitated

from D.Mavis, MRC
What about 130nm CMOS and beyond?

- Measurements in 130nm (3 manufacturers) and 90nm (preliminary, 1 manufacturer) available
- Radiation performance most often improved
- In the CERN selected Foundry, baseline for logic is use without ELTs and guardrings (commercial library)
- For both logic and analog, a document is available summarizing results and recommendations. This is available for designers in “agreed” Institutes – users of the selected technology with valid NDA in place. Contact me to get this document.
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SEU and scaling

- $V_{DD}$ reduced
- Node C reduced
- New mechanisms for SEU

All points to an increased sensitivity!

✓ In commercial products, in reality the situation has been measured not to be that bad (so far...). DRAM have been getting actually better, whilst SRAM worse per chip (due to increase in memory cells per chip)

✓ Not only $V_{dd}$ and node capacitance have to be taken into account: sensitive area and charge collection efficiency are also important and change with technology generation!
SEL and scaling

- Retrograde wells
- Trench isolation
- $V_{DD}$ reduced

All these issues help in preventing SEL, but they might not be always effective.
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Solutions: SEU

- Technology level: epitaxial substrates, SOI,…
- **Cell design: SEU-tolerant FFs or memories**
- Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- **Always to be considered at system level**
Cell design (1)

- Increase the critical charge by increasing the node capacitance:
  - Design larger transistors – also more driving strength
Cell design (2)

- Increase the critical charge by increasing the node capacitance:
  - Add “extra” capacitors
    - Metal/metal to avoid losing space

Upset rates in proton environment:
- Twofold decrease for the “oversized”
- Tenfold decrease for the “overloaded”
Cell design (3)

- **DICE (Dual Interlock Cell)**
- Dual Interlock ensures SEU protection against hit on one node
- Writing in the cell requires access to 2 nodes
Cell design (4)

✓ **DICE** cell weakness:

- Recovery time needed after SEU
  - Output glitch
  - A rising edge of the clock during recovery time can store wrong data in the following pipeline stage
- Local clock buffers
- Charge collection by multiple nodes is not negligible! (in 90nm technology, just 10x SEU rate improvement)
Cell design (5)

- Use special cell architectures
  - Temporal sampling with internal clock delays (after Mavis) effective against digital SET

- Transient can only be captured by 1 latch
- Sensitive to transients on clock line
- Many variations to this concept exist (one can delay data instead of clock, for instance)
Solutions: SEU

- Technology level: epitaxial substrates, SOI,…
- Cell design: SEU-tolerant FFs or memories
- Redundancy
  - Triple Modular Redundancy (TMR): triplication and voting
  - Encoding (EDAC)
- Always to be considered at system level
Redundancy: TMR (1)

- Triplication with 1 voter

- The state machine is instantiated 3 times, with 1 voter
- An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
- An error in the voter instead corrupts the state!
Redundancy: TMR (2)

- Triplication with 3 voters
  - The state machine is instantiated 3 times, with 3 voters
  - An SEU can corrupt the output of one of the blocks, but majority voting restores the correct state
  - An error in one of the voters is also restored
  - This seems a lot of additional transistors, but sometimes the designer can find more “compact solutions”. This is shown in the following example.
A majority voter can necessitate a large number of transistors. Since 3 voters are required to protect the data from errors in the voter, the overall area penalty can be very large!

One compact solution for the voter is in the schematic below:

- Very compact layout
- 14 transistors (better than XOR+MUX style)
- Fast
  - 2 logic levels only
  - Possible to save the inverter (2 transistors less)
- Still 3 voters are needed, for a minimum of 36 transistors
Example of TMR in registers (2)

- To save some transistors, it is possible to merge the voter in the register, and make a single cell.
- Each “super cell” will then have 3 inputs and 1 output with merged connections between them.

Diagram:

- Three registers are shown with majority voters.
- Each majority voter has 3 inputs (D0, D1, D2) and 1 output (Q).
- Connections are shown between the inputs and outputs of the majority voters.
- The output of each register is connected to the input of the next register.
- The clock signal (ck) is connected to the input of each register.
- The diagram illustrates the TMR (Triple Modular Redundancy) configuration for registers.
Merging of the voter can be done at different levels.

The example below, for a dynamic FF, illustrates it. The first part of the FF cell is shown in the left picture, with its timing diagram.

A first level of merging is achieved by integrating the voter in the input inverter, as shown in the right picture. This does not really save transistors with respect to a separate voter.
A “deeper” merging, where the voter is moved inside the FF, leads to considerable area saving.

This integration of the voter in the cell “only” costs 5 additional transistors! For 3 “super cells”, the penalty for the voter decreases from 36 to 15 transistors!
Solutions: SEU

✓ Technology level: epitaxial substrates, SOI,…
✓ Cell design: SEU-tolerant FFs or memories
✓ Redundancy
  • Triple Modular Redundancy (TMR): triplication and voting
  • Encoding (EDAC)
✓ Always to be considered at system level
Redundancy: encoding (1)

- Adding redundant information (bits) and encoding-decoding
  - Used for data transmission and for memories
  - Requires complex encoding-decoding logic
  - Several different codes can be used (Hamming, Reed-Solomon, BCH, etc.)

Encoder → Memory array (each word with redundant bits) → Decoder
Redundancy: encoding (2)

✓ Example: Hamming encoding (1950)

- $k =$ number of message bits
- $q =$ number of check (parity) bits
- $n =$ number of word bits

Minimum distance between words = 3
⇒ All valid words in the code differ AT LEAST by 3 bits
⇒ It can be used for single error correction, double error detection

\[ n = k + q \quad n \leq 2^q - 1 \]
Redundancy: encoding (3)

Example: Hamming encoding (1950)

Example of encoding for $k = 8$ $q = 4$ $n = 12$

Encode in a way requiring “as easy as possible” encoding/decoding logic

1. Check bits in powers of 2 positions in the word (position 1, 2, 4, 8)
2. Other word bits are the message bits
3. Each check bit computes the parity for some of the word bits:
   - Position 1: check 1 bit, skip 1 bit, etc. (bits 1, 3, 5, 7, 9, 11)
   - Position 2: check 2 bits, skip 2 bits, etc. (bits 2, 3, 6, 7, 10, 11)
   - Position 4: check 4 bits, skip 4 bits, etc. (bits 4, 5, 6, 7, 12)
   - Position 8: check 8 bits, skip 8 bits, etc. (bits 8, 9, 10, 11, 12)

Word to encode: 10101010

$\begin{array}{ccccccccc}
\text{word} & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 \\
\text{position} & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12
\end{array}$
Redundancy: encoding (4)

Example: Hamming encoding (1950)

Word to encode: 10101010

Encoded word: 11110100101010

Position: 1 2 3 4 5 6 7 8 9 10 11 12

SEU changes to: 11110000101010

Check the parity bits in the received word:
- Position 1: OK
- Position 2: wrong
- Position 4: wrong
- Position 8: OK

The position of wrong bit is the sum of the wrong positions, that is Position 6!
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Reducing SEL sensitivity

The best solution is to decrease the gain of the parasitic pnpn structure. Technological and layout solution can help in that respect:

Technological
- => use of epitaxial substrates and retrograde wells
- => use of trench instead of junction isolation

Layout
- => increase the distance between complementary devices
  => use guardrings
  => use lots of substrate and well contacts
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- In state-of-the-art commercial-grade CMOS technologies, reliable radiation tolerance can be achieved with HBD techniques.
- If “natural” TID is insufficient, the use of ELTs and guardrings can “upgrade” it – large effort needed mainly for digital design.
- SEU rates can be decreased with proper engineering (study of environment, introduction of tolerant cells, redundancy, encoding, etc.) and should always be considered at the system level.
- SEL – already unlikely – can be further controlled by careful layout.
To study further radiation effects

✓ General material on radiation effects:
  - The best source is the “archive of Radiation Effects Short Course Notebooks, 1980-2006” collecting the courses given at the IEEE NSREC conference (CD sold by IEEE)
  - “Classic” books on the subject
  - Recent Books with good overview of all effects:
  - Best papers from the Nuclear and Space Radiation Effects Conference (NSREC) are published yearly in the IEEE TNS in the december special issue

✓ Specialized conferences:
  - NSREC in the US, yearly in July
  - RADECs in Europe, conference (1 week) or workshop (2-3 days) every year in September
Further reading on HBD

- **On Enclosed Transistor Layout:**
  - Ph.D. thesis describing results in 0.25μm technology:

- **On SEU-tolerant Cells:**
  - Increased capacitance:
    - F.Faccio et al., "SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25mm CMOS technology for applications in the LHC", in the proceedings of the Fifth Workshop on Electronics for LHC Experiments, Snowmass, September 20-24, 1999, pp.571-575 (CERN 99-09, CERN/LHCC/99-33, 29 October 1999)
  - Special SEU-tolerant cells:

- **On TMR and encoding:**