MTest Pixel Telescope Status

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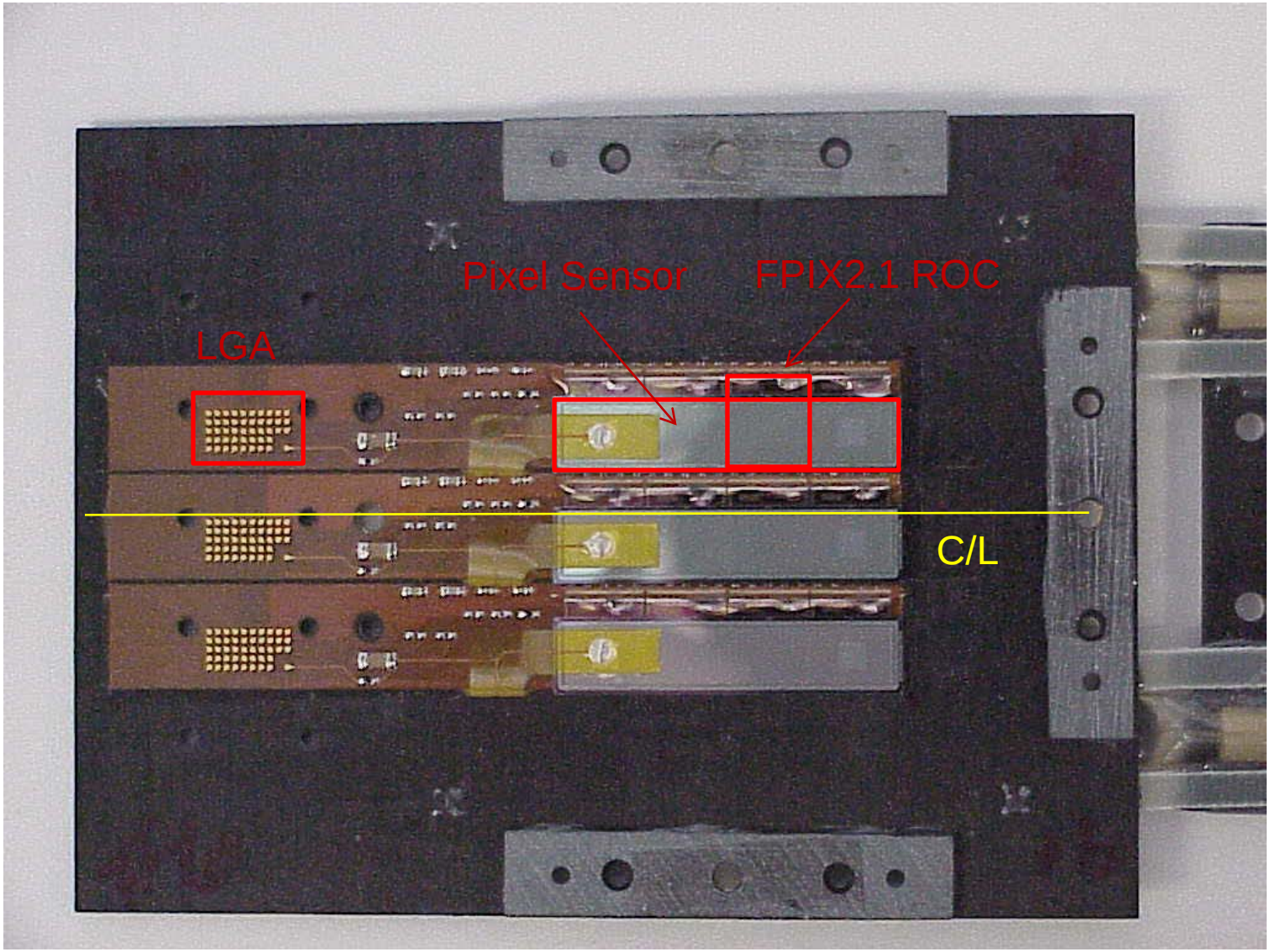
Pixel Detector Highlights

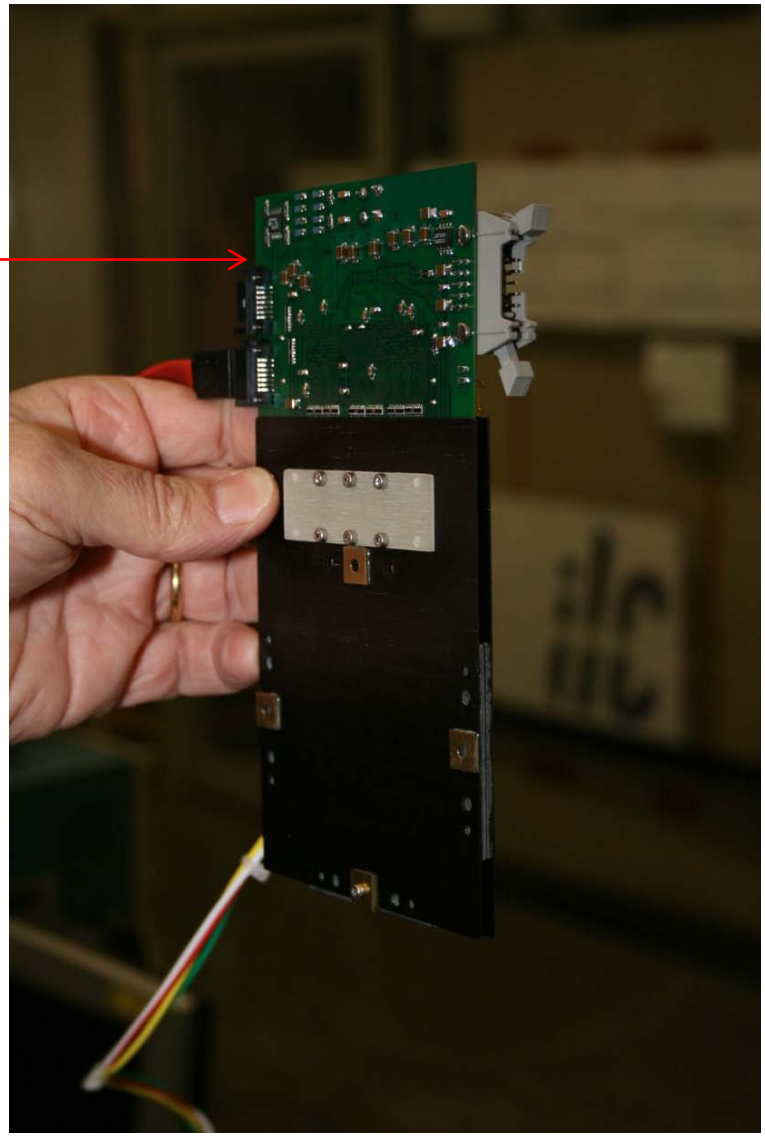
- Each station consists of 6 BTeV “4x” modules.
  - 50μ x 400μ pixels → station is either precision-x or precision-y.
  - 2 planes of 3 modules each facing one another with an offset to provide ~3.5 cm x 3.5cm coverage.
  - Each sensor is bump bonded to 4 FPIX2.1 ROCs.
  - Bump bonded hybrid is glued to Kapton flex circuit (HDI) & ROCs wire bonded to HDI.
  - 0201 surface-mount caps & resistors next to ROCs minimize number of traces required for HDI.
  - HDI I/O is through a Land Grid Array

Pixel Plane (1/2 Station)

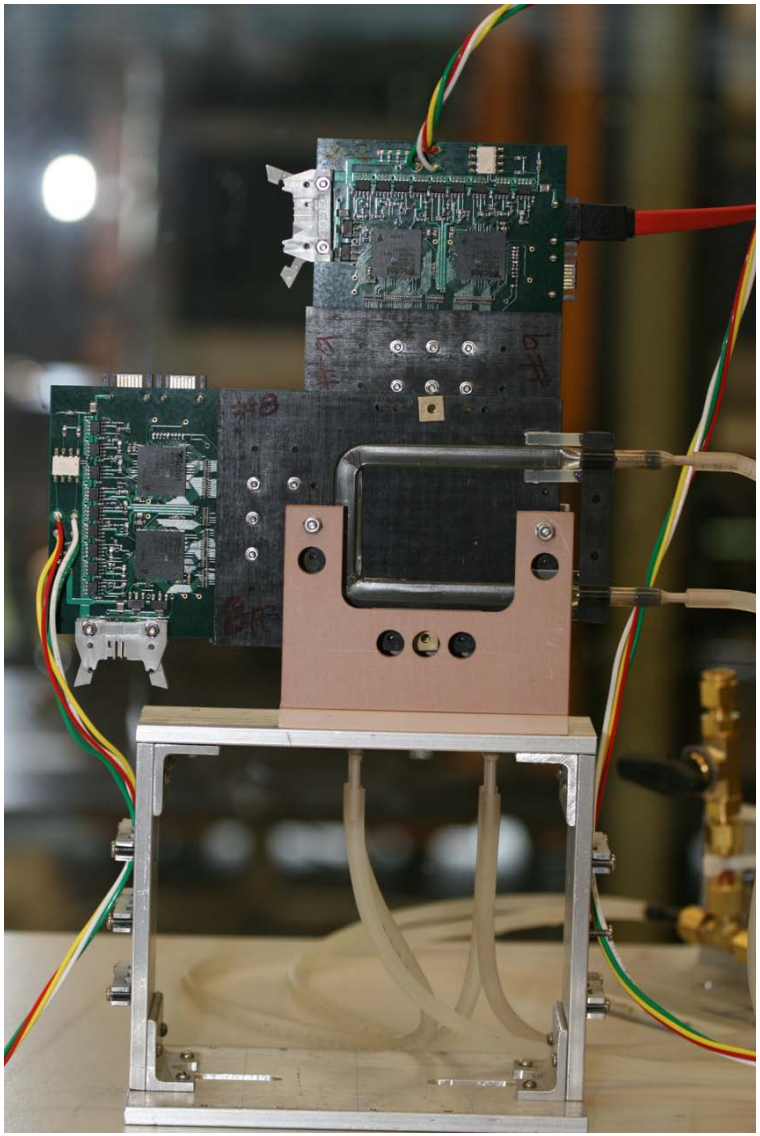


Pixel Station

Readout Card
(TBDB)



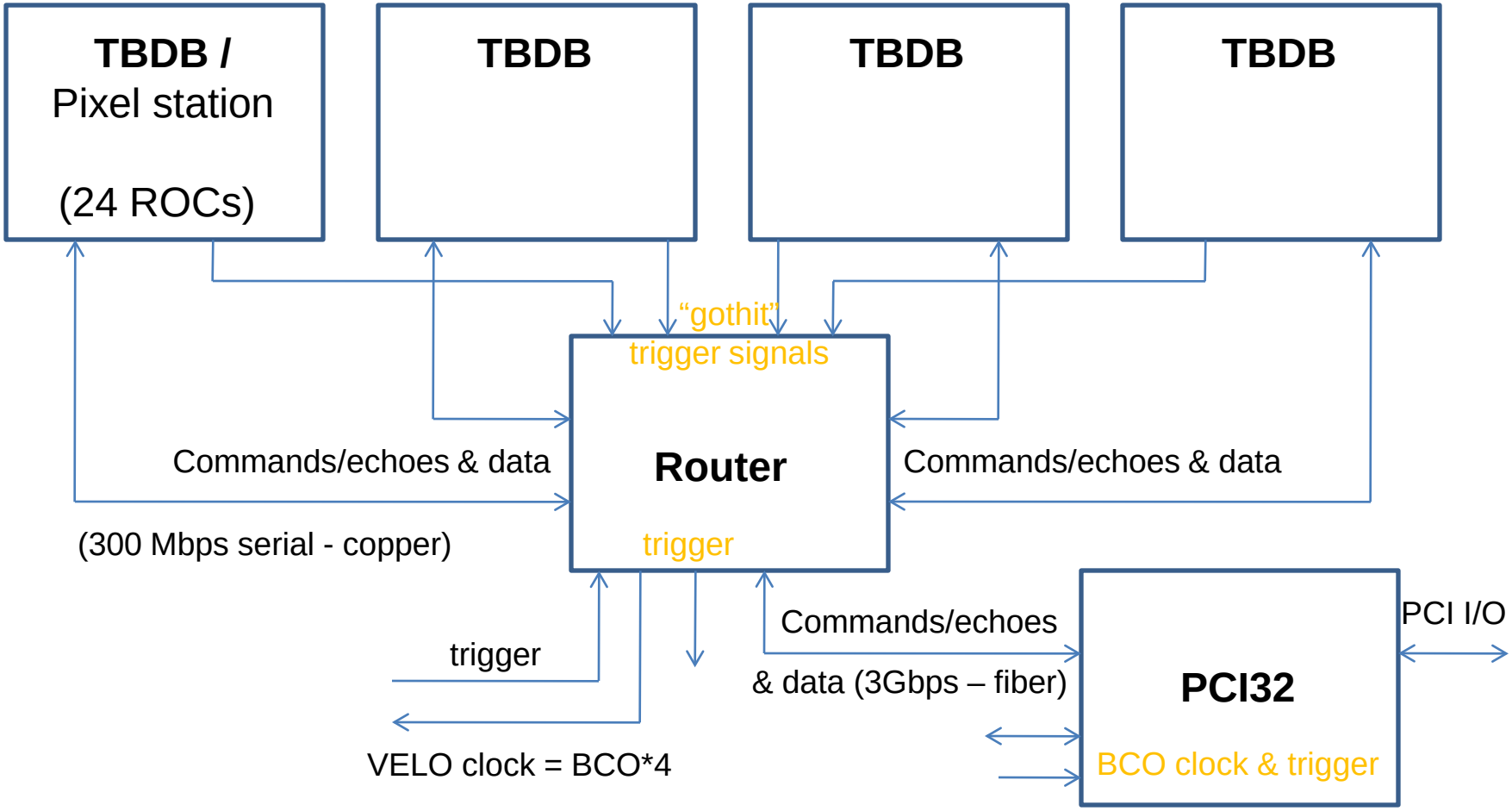
Pixel Double Station



DAQ Overview: Software

- Interface is both a PCI master & slave.
  - Controlled by registers, status recorded in registers.
  - Uses 64 MB of PC memory – available to user programs via LINUX memory map.
  - Memory organized into 3 ring buffers:
    - Outgoing commands
    - Command echoes / read register results
    - Pixel data
- Multiple independent processes can access buffers.
  - Accommodates many coding styles/languages
  - Recent data taking used my (FORTRAN) programs to initialize & monitor pixel ROCs & sensors & JC's (C & C++) programs to collect data & find tracks.

DAQ Overview: Hardware



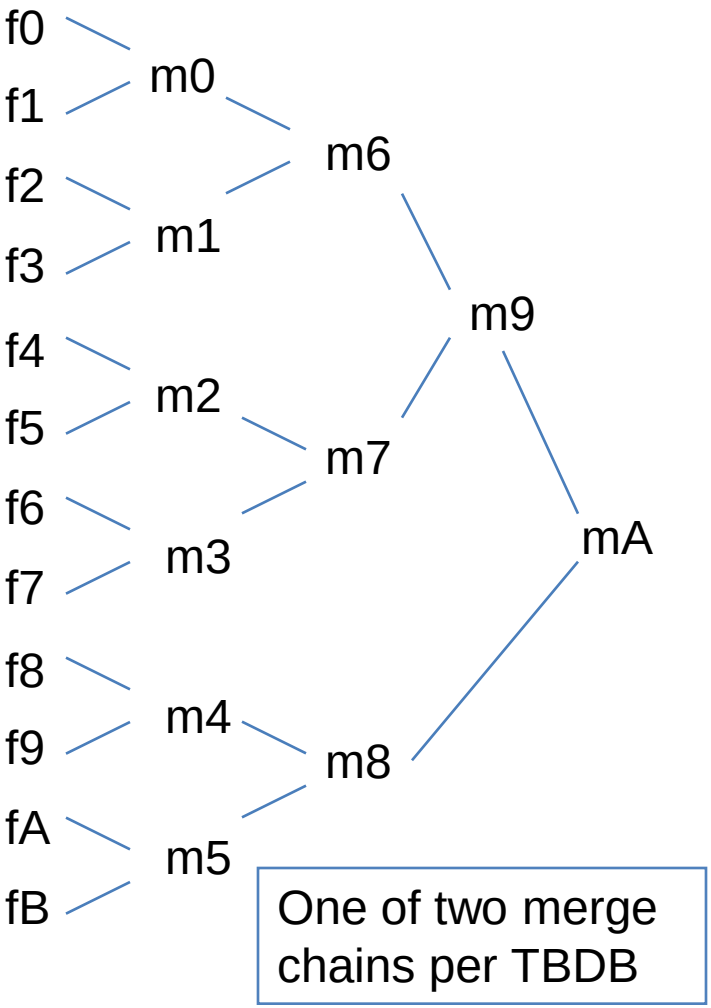
Data Flow: Pixel module to TBDB

- Each FPIX2.1 chip sends (24-bit = bco,row,col,adc) data serially on one differential pair. When no data exists (and each time a readout scan is completed) a synchronization & status word is output.
- A TBDB receives information from 6x4=24 FPIX2.1 chips simultaneously. Each input uses a “digital phase follower” (4x oversample) to determine the input phase. Status information is output only in response to a request.
- Each input ensures that the data is time ordered (using two FIFOs) and constructs packets of 16-bit words: FW(12-bit bco), FW(chipid), 15-bit data(row,col,adc), 15-bit data…

Data Flow: Two FPGAs per TBDB

- Each FPGA receives data from 12 FPIX2.1s. Data streams are merged two at a time: at each stage, if information is present at both inputs, the packet with the earlier bco time is selected first.

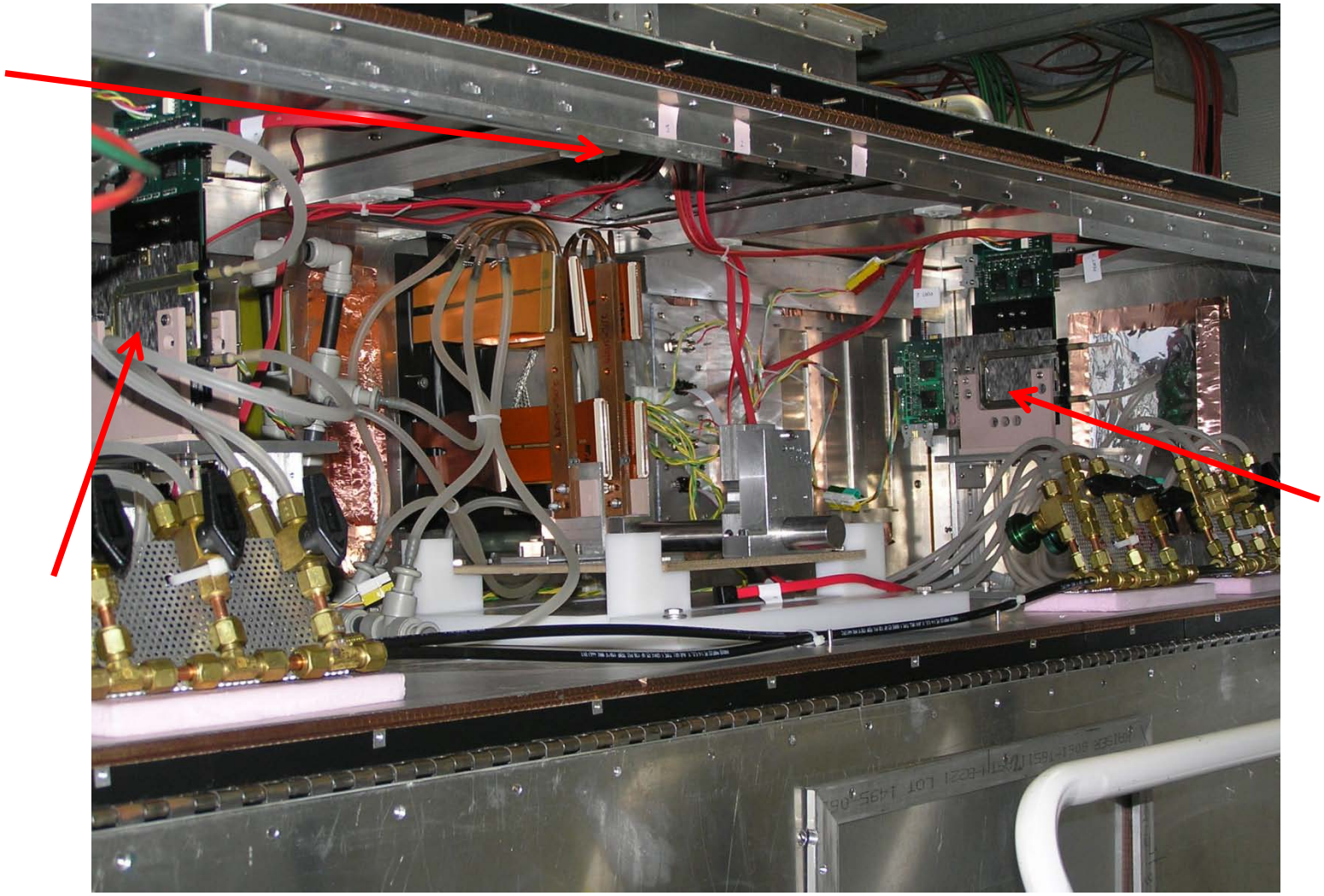
- Chipid is modified at each merge by shifting the ID field right one bit & setting the high order bit to 1 for data from input #1. The final chipid reflects the data path through the merges.



Data Flow: TBDB to Router

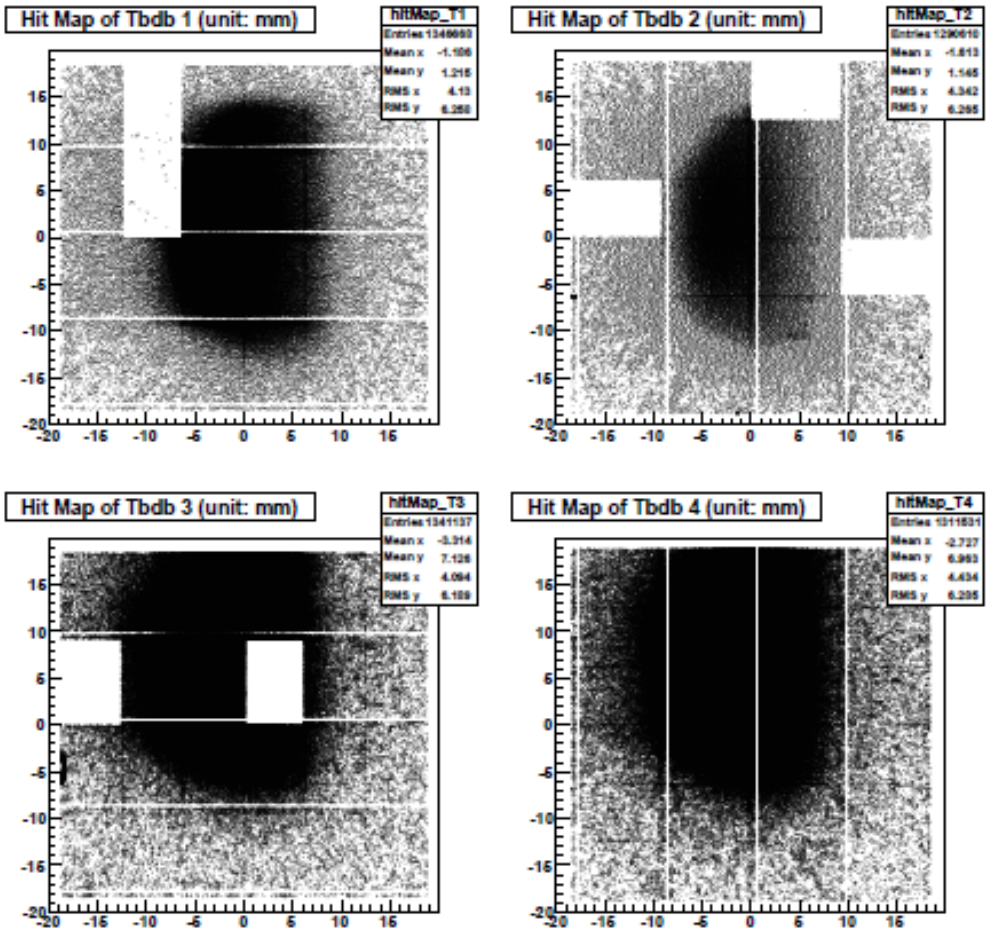
- Data from the two FPGAs on a TBDB is merged in another 2-way merge; the same shift & tag operation is performed on every chipid FW.
- Data from up to six TBDBs is input to the Router.
- The router can also receive an external trigger pulse; it forms a trigger packet that looks similar to a pixel data packet: FW(12-bit bco), FW(trig+ 4 more bco bits), 12-bit trigger #.
- Pixel and trigger data packets are merged in 2-way merges & output to the DAQ computer (pci interface).
- A Last Word(LW) is added by the router (repeating the bco#) at the end of each fully formed packet.

Pixel Tracker (telescope) in MTest



Beam Spots – Friday 2/20/09 16:25-17:00

~1.3M entries



Upstream station pair

Downstream station pair

White stripes are plotting artifacts; white rectangles are readout chips w/noisy pixels that were disabled for this data (won't need to be disabled in the future).

Status & Immediate Plans

- Major readout problems (hangs) have all been resolved.
- Minor problems (loss of commands/echoes) being debugged.
  - Can work around these problems.
- One more pixels-only run planned.
  - nominally 3/16 – 3/21.
- VELO (LHCb) test in April if possible.
- Tests of thin edgeless pixel sensors.

Longer term plan

- Add one high-precision station.
  - LBL-supplied “MIMOSA-V” MAPS?
    - Rolling shutter readout.
    - 2-3 μ resolution.