

Summary of FPIX tests

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- Pixel input feeds a charge integrator followed by X4 gain stage
- Gain stage output feeds 8 comparators
- 8 comparator thresholds, each programmed with a DAC
- All DACs referenced to one master bias current (set with external R)
- Vref DAC sets DC operating point of 2nd stage
- $(V_{dda}) - (\text{operating point of 2}^{\text{nd}} \text{ stage})$ determines DC bias point of comparators

Master Bias Options

- **Option 1:** Refres resistor to ground
- Master current determined only by diode drop voltage level
- Master current stable, insensitive to V_{dda}
- Most bias levels and reference voltages are stable and insensitive to V_{dda}
- Comparator bias current quite sensitive to V_{dda}
- **Option 2:** V_{master} resistor to ground
- Some dependence of master current on parameter variation, V_{dda} .
- Most bias levels and reference voltages are mildly dependent on V_{dda}
- Comparator bias current much **less** sensitive to V_{dda}
- **USE OPTION 2**

Master bias option 1

Rbias1	Vdd - Vref	Iavdd (total)	Vref - Vth0	(Δ Vth)/(DAC count)
561K	0.654 V	65 mA	172 mV	9.2 mV
585K	0.734 V	75	165	8.7
618K	0.832 V	90	156	8.2

With Rbias1 = 585K, vary Vdda:

Vdda	Vdd - Vref	Iavdd (total)	Vref - Vth0	(Δ Vth)/(DAC count)
2.4	0.639 V	60 mA	165 mV	8.7 mV
2.5	0.734 V	75	165	8.7
2.6	0.834 V	90	165	8.7

Comparator bias varies significantly with Vdda

Threshold very stable

Master bias option 2

Rbias1	Vdd - Vref	Iavdd (total)	Vref - Vth0	(ΔV_{th})/(DAC count)
1.382 Meg	0.71 V	75 mA	170 mV	8.5 mV
1.440 Meg	0.78 V	80	161	8.5
1.500 Meg	0.84 V	90	154	8.2

With Rbias1 = 1.44Meg, vary Vdda:

Vdda	Vdd - Vref	Iavdd (total)	Vref - Vth0	(ΔV_{th})/(DAC count)
2.4	0.771 V	75 mA	152 mV	8.1 mV
2.5	0.776 V	80	161	8.5
2.6	0.781 V	85	170	9.0

Comparator bias varies little (desirable!)

Threshold varies somewhat (OK)

Biasing for FFR stability

- Doing “FFR” reset with previous resistor bias values can result in oscillation (reason for this discussed later)
- Select revised Vmaster resistor of 910K (1%) to avoid FFR oscillation (second stage and comparators are completely debiased)
- All nominal DAC values must be recomputed and programmed
- With 910K bias, Vref and comparator thresholds are about 12 mV/count (this can vary chip to chip)
- If FFR cannot be done due to oscillation at power-up (which causes Vddd drop due to current limiting), then: Set Vdda = 0 (which reduces the Vddd supply current), perform FFR, program desired register values, and then restore Vdda.

Gain and calibration issues

- Sensor capacitance (pixel input to HV backplane) is consistently 10 fF.
- FPIX charge gain is determined by integrator feedback capacitance
- Integrator feedback C is made from ILD parasitic: not well controlled!
- Large variation in charge gain from chip to chip (I saw anywhere from 290 mV/fC to 500 mV/fC!
- Test pulse input C has the same uncertainty
- The only way to calibrate a chip's charge gain is to inject a known charge through the 10 fF sensor capacitance, by applying a known step voltage to the sensor backplane.
- Perhaps each chip should be calibrated during test?

Comparator DC bias issues

- Very important since it affects stability (discussed later)
- Measure the comparator bias current for different Vref DAC settings on one chip. This bias current will affect the comparator delay.
- The chip measured has the lowest comparator bias current of all 8 chips on the tested module, for a given Vref setting. I measured a 50% spread in comparator bias currents (for a given Vref) over the 8 chips.

Vref DAC	Vdda - Vref	Ibias per comparator
138	0.65 V	0.13 uA
135	0.69 V	0.17 uA
130	0.75 V	0.35 uA
125	0.81 V	0.58 uA
120	0.87 V	0.87 uA
115	0.93 V	1.22 uA
110	0.99 V	1.62 uA

Comparator delay/timewalk

- Approx. 12 mV/(DAC count)
- Set threshold (V_{th0}) to 10 counts below V_{ref}
- Threshold offset of several counts
- Effective threshold is therefore about 1400 e
- Chip charge gain is 340 mV/fC
- Desired V_{ref} 120 – 125 counts? (Comparator bias ~ 0.8 μ A)

Input = 1600 e

V_{ref} DAC	V_{th0} DAC	Delay from threshold crossing
125	115	---
120	110	---
115	105	99 ns
110	100	78 ns

Input = 1800 e

V_{ref} DAC	V_{th0} DAC	Delay from threshold crossing
127	117	---
125	115	176 ns
120	110	111 ns
115	105	89 ns

Input = 2000 e

Vref DAC	Vth0 DAC	Delay from threshold crossing
133	123	---
130	120	186 ns
125	115	119 ns
120	110	83 ns
115	105	61 ns

Input = 2400 e

Vref DAC	Vth0 DAC	Delay from threshold crossing
>141		---
141	131	275 ns
135	125	169 ns
130	120	119 ns
125	115	85 ns
120	110	68 ns
115	105	54 ns

Input = 3600 e

Vref DAC	Vth0 DAC	Delay from threshold crossing
135	125	93 ns
125	115	57 ns
115	105	42 ns

Input = 7200 e

Vref DAC	Vth0 DAC	Delay from threshold crossing
135	125	60 ns
125	115	43 ns
115	105	33 ns

Stability problems

- Several positive feedback paths exist
- Feedback strength depends on several factors, some under our control and some not

Instability due to DAC leakage current

- Thousands of DAC sections driven by master reference
- Each section has I_{leak} due to digital switch
- Leakage current into switch depends on $(V_{dda} - V_{ddd})$
- If $V_{dda} > V_{ddd}$, leakage is big enough to subtract significantly from master reference current, lowering V_{ref}
- Lower V_{ref} to the 2nd stage increases the comparator bias current. This reduces on-chip V_{dda} due to parasitic supply bus resistance, which lowers V_{ref} even more: positive feedback!
- Solutions:
 - always set $V_{dda} = V_{ddd} - 0.2V$
 - Bypass V_{ref} to ground with at least 0.1 μF

AC instability

- Feedback paths from comparators back to integrator through common parasitic resistance in both ground and Vdda busses, and capacitance from ground and Vdda to the integrator input
- Factors affecting feedback strength:
 - Comparator gm (depends on comparator bias **and** # of sections used)
 - Parasitic R in ground supply bus (shunted somewhat by substrate)
 - Parasitic R in Vdda supply
 - Parasitic C from Vdda to integrator input
 - Sensor C from external ground to integrator input
 - Integrator feedback C
- Substantial chip to chip variation in several of these quantities!!
- Unavoidable chip to chip variation in sensitivity to oscillation

“Best” configuration

- $V_{dda} = 2.3V$, $V_{ddd} = 2.5V$
- Bias with 910K from V_{master} to ground (no V_{ref} resistor)
- 0.1 μF or bigger bypass from V_{ref} to ground
- 0.1 μF or bigger bypass from V_{bp1} to ground
- 0.1 μF or bigger bypass from V_{th0} to ground (for threshold stability)
- Minimize V_{dda} and ground resistance on HDI
- 0.01 μF bypass cap from V_{master} to V_{dda} (for ESD protection only).
Note this cap must be at least a factor of 10 smaller than the V_{ref} bypass to avoid oscillation through the path described by the leakage current problem
- Suggested DAC settings (?): $V_{ref}=122$, $V_{th0}=112$, $V_{fb2}=103$,
 $I_{bp1}=0$, $I_{bp2}=0$, $I_{bb}=18$, $I_{ff}=8$

Stability tests for 8-chip module

- As soon as any one chip begins to oscillate, the whole module oscillates
- Look at module stability as a function of:
 - how many of the 8 comparators are enabled
 - Vref setting
 - how many chips are enabled

3 comparators on

Chips enabled	Min. Vref
1	118
2	118
3	116
4	114
5	115
6	112
7	114
8	122
1-8 (all)	135
1-7	122
4,5,6,7	118
4,6,7,8	126
6,7,8	126
4,6,7	117

- 8-chip HDI with sensor: measure minimum Vref that avoids oscillation
- On this particular module, chip #8 is most sensitive to osc.
- When multiple chips are enabled, the min. Vref is several counts higher than the most sensitive individual chip
- Safe Vref setting would be well above the min. Vref

8 comparators on

Chips enabled	Min. Vref
1-8 (all)	147
1-7	137
8	138
4	130

4 comparators on

Chips enabled	Min. Vref
1-8 (all)	139
1-7	127
8	126
4	120
4,5,6,7	124
4,5,6,8	135

2 comparators on

Chips enabled	Min. Vref
1-8 (all)	130
1-7	113
8	122
4	104

1 comparator on

Chips enabled	Min. Vref
1-8 (all)	100 (not consistent)
8	100
4	84

Conclusions

Proper biasing, bypassing, etc. can help immunity to oscillation, but by far the 2 most important factors are:

- comparator bias current
- # of comparators used

At present, we have tested only one 8-chip module with a sensor. There is significant chip to chip variation in sensitivity to oscillation. The sensitivity of the module as a whole is determined by the weakest chip.

With a reasonable comparator bias current, operating one comparator seems safe, but using more than one comparator is not!!

Separating the integrator and comparator supply nets should solve this problem, but would require a new run.