# Design and Testing of Monolithic Active Pixel Sensors for Charged Particle Tracking

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***Abstract*—A Monolithic Active Pixel Sensor (MAPS) for charged particle tracking based on a novel detector structure has been proposed, simulated, fabricated and tested. This detector is inseparable from the readout electronics, since both of them are integrated on the same, low-resistivity silicon wafer standard for a CMOS process. The individual pixel is comprised of only three MOS transistors and a photodiode collecting the charge created in the thin undepleted epitaxial layer. This approach provides a low cost, high resolution and thin device with the whole detector area sensitive to radiation (100% fill factor). Detailed device simulations using the ISE-TCAD package have been carried out in order to study the charge collection mechanism and to validate the proposed idea. In order to demonstrate viability of the technique, two prototype chips were successively fabricated using 0.6 $\mu$m and 0.35 $\mu$m CMOS processes. Both chips have been fully characterized. The pixel conversion gain has been calibrated using a $^{55}$Fe source and prototypes have been exposed to a 120 GeV/c pion beam at CERN. The final test results with emphasis on the first prototype are reviewed. The experimental data is preceded by general design ideas and simulation results.**

***Index Terms*—Active pixel sensors, CMOS processes, conversion gain calibration, device modelling, particle tracking, pixel detectors, silicon position sensitive detectors, simulation.**

## I. Introduction

THIS paper presents a novel position sensitive device for charged particles tracking and imaging—the Monolithic Active Pixel Sensor (MAPS)—which integrates on the same substrate the detector element and the processing electronics. The baseline architecture of the proposed device is similar to a visible light CMOS camera, emerging recently as a substantial competitor to standard CCDs for digital photography and video applications [1]. Until now, several attempts were made to combine detector and electronics onto the same substrate [2], [3], but all of them used high-resistivity silicon as the fully depleted active volume. This approach is optimized for the charge collection efficiency, but complicates the detector design since a dedicated fabrication process is required. Charge collection can also be achieved when a lightly doped undepleted epitaxial layer is used as an active volume [4], [5]. The epitaxial layer is available in numerous modern very large-scale integration (VLSI) processes featuring twin tubs, where it is grown on a highly, usually p-type doped substrate. The presented solution takes advantage of the epitaxial layer and, unlike the previously proposed monolithic tracking devices, the new device can be fabricated using a standard, cost-effective and easily available CMOS process. The charge generated by the impinging particle is collected by the n-well/p-epi diode, created by the floating n-well implantation reaching the epitaxial layer. This structure forms potential well attracting electrons. The active volume is underneath the readout electronics allowing a 100% fill factor, as required in tracking applications.

In order to validate these ideas, two prototype chips were fabricated using 0.6 $\mu$m and 0.35 $\mu$m CMOS processes. The design principle is reviewed in the next section and physics device simulations are discussed in the consecutive part. The last section gives an overview of the experimental results with the emphasis on the beam tests data analysis.

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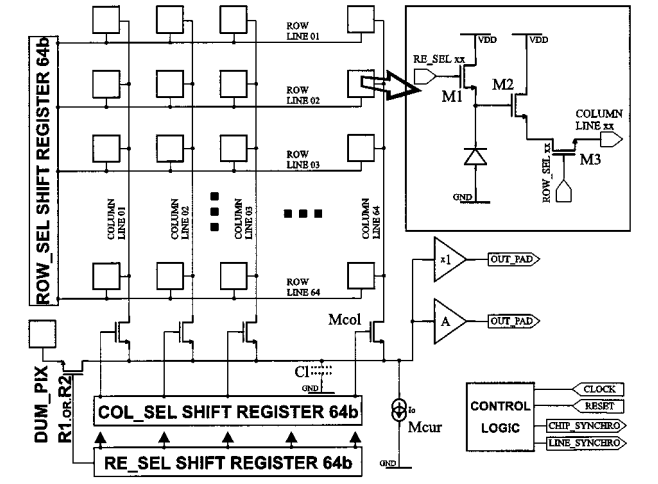
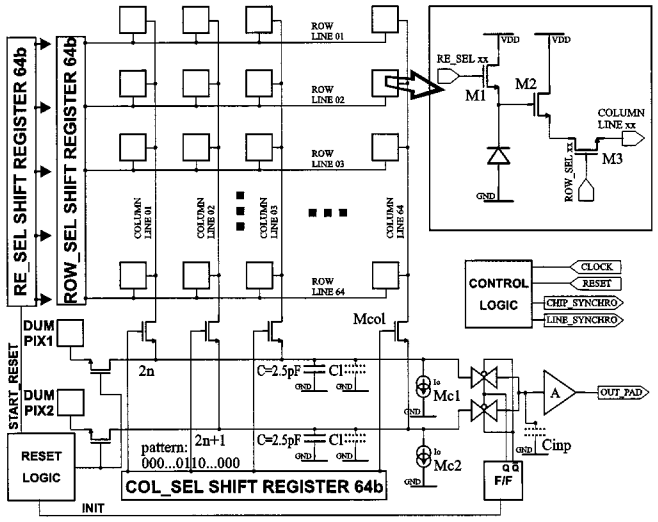
## II. Detector Architecture

### A. General Design Guidelines

Two prototype Minimum Ionizing particle MOS Active pixel sensor (MIMOSA) chips, following the presented idea, were fabricated in two different processes. The first device MIMOSA I was fabricated in a 0.6 $\mu$m process featuring an epitaxial layer of about 14 $\mu$m and the second chip, MIMOSA II, was fabricated in a 0.35 $\mu$m process with less than 5 $\mu$m of this layer. Both chips contain several (four and six in the case of MIMOSA I and MIMOSA II, respectively) independent arrays of active elements having slightly different design. Each array is made of 64 by 64 square pixel elements, laid down with a pitch of 20 $\mu$m in both directions. The individual pixel is comprised of only three MOS transistors and a floating diffusion photodiode. Because the n-well implantation areas are used for the collecting diodes, the design is limited to NMOS transistors only at the pixel level, whereas both types of transistors are used on the chip periphery. Chips are equipped with a serial analogue readout, requiring only two digital signals to operate. Such a simple readout arrangement used in both small-scale detector chips, allowed easy operation of the device and was sufficient for demonstrating feasibility of the new detection technique. It is worth noting that in future designs the readout will be optimized to satisfy specific requirements related to each application. For example, adding parallel column-wise data handling or including some data processing directly on a chip will improve substantially the readout speed.




(a)




(b)

Fig. 1. Schematic diagrams of MIMOSA I (a) and MIMOSA II (b) chips.

The schematic diagrams of MIMOSA I and II are presented in Fig. 1. The transistor M1 resets the photodiode to reverse bias, the transistor M2 is a source follower combined with the current source Mcur, which is common to the entire column, while the transistor M3 combined with Mcol is used to address the pixel for readout. Periodically, the floating diffusion of the collecting diode has to be reset to remove the collected charge and to compensate the diode leakage current. This procedure superimposes thermodynamic fluctuations onto the signal described statistically by

$$\langle V_n^2 \rangle = \frac{kT}{C_d} \tag{1}$$

where $C_d$ is a node capacitance, $k$ is the Boltzman constant and $V_n$ represents the noise voltage.

This type of noise dominates the contributions from other sources and is known as the kTC noise. It can be removed applying correlated double sampling (CDS) signal processing [6]. For both circuits, the CDS operation is performed by software during offline data processing [5] and the useful signal is calculated as the difference between two consecutive frames taken after the reset. The detector operated in this mode is a charge-integrating device with an integration time equal to the readout time of one full frame, given by

$$\tau_{\text{int}} = N_p (f_{\text{clk}})^{-1} \tag{2}$$

where $N_P$ is the total number of pixels connected to one serial output line and $f_{\text{clk}}$ is the readout clock frequency. Two 64 bit long shift registers, selecting rows and columns, are used for pixel addressing. The analogue information is read out with consecutive clock cycles. The array is reset in 64 clock cycles, when the reset shift register selects the entire row at a time.

The bias current of the on-pixel source follower is a trade-off between the noise performance and the readout speed. The reduced bias current in combination with the column line parasitic capacitance decreases the cutoff frequency of the source follower. The bandwidth was restricted in the maximum extent preserving assumed readout speed, although its optimum adaptation to the full frame interval CDS was not possible. A special technique allowing more restrictive bandwidth limiting preserving fast readout was implemented in MIMOSA II. Two separate readout lines with two current sources inside the chip are switched alternatively to the output amplifier by two transmission gates. All even columns are connected to the first line and all odd columns to the second one. When a chosen column is selected for readout, the neighboring one is being prepared by connecting the bias current. Both readout lines are loaded with additional capacitance of 2.5 pF, limiting the bandwidth of the source follower and improving the noise performance. The input capacitance of the output amplifier is small enough to be charged quickly after the transfer gate is activated. This technique, combined with an optimized design of the output amplifier, allows increasing the readout frequency up to 25 MHz, to be compared to 5 MHz in the case of MIMOSA I.

### *B. Design Details*

The basic configuration for both chips features one collecting diode per square pixel with all transistors designed in a standard rectangular form. This default topology is depicted in Fig. 2(a). The second characteristic configuration of MIMOSA I is a design with four collecting diodes placed close to each pixel corner and short-circuited to the common source follower gate [Fig. 2(a)]. This configuration reduces the charge collection time and the charge spreading among neighboring pixels, at the expense of increased noise due to the higher node capacitance (decreased charge-to-voltage conversion gain).

There are two new features implemented in MIMOSA II. In order to optimize the signal-to-noise ratio for reconstructed clusters, a staggered pixel layout was introduced [Fig. 2(c) and (d)], where every other row is shifted by half the pixel pitch. In this way each pixel has only six closest neighbors, reducing potentially the number of pixels in a reconstructed cluster.

Since the radiation environment of many applications will be harsh, the radiation hardness of the new devices is an important issue. Therefore, array configurations shown in Fig. 2(c), 2(d), and also the second version of Fig. 2(a) were designed in radiation tolerant geometry with enclosed NMOS transistors [7]. The charge collection efficiency of four collecting diodes was traded for a better charge-to-voltage conversion factor. A configuration

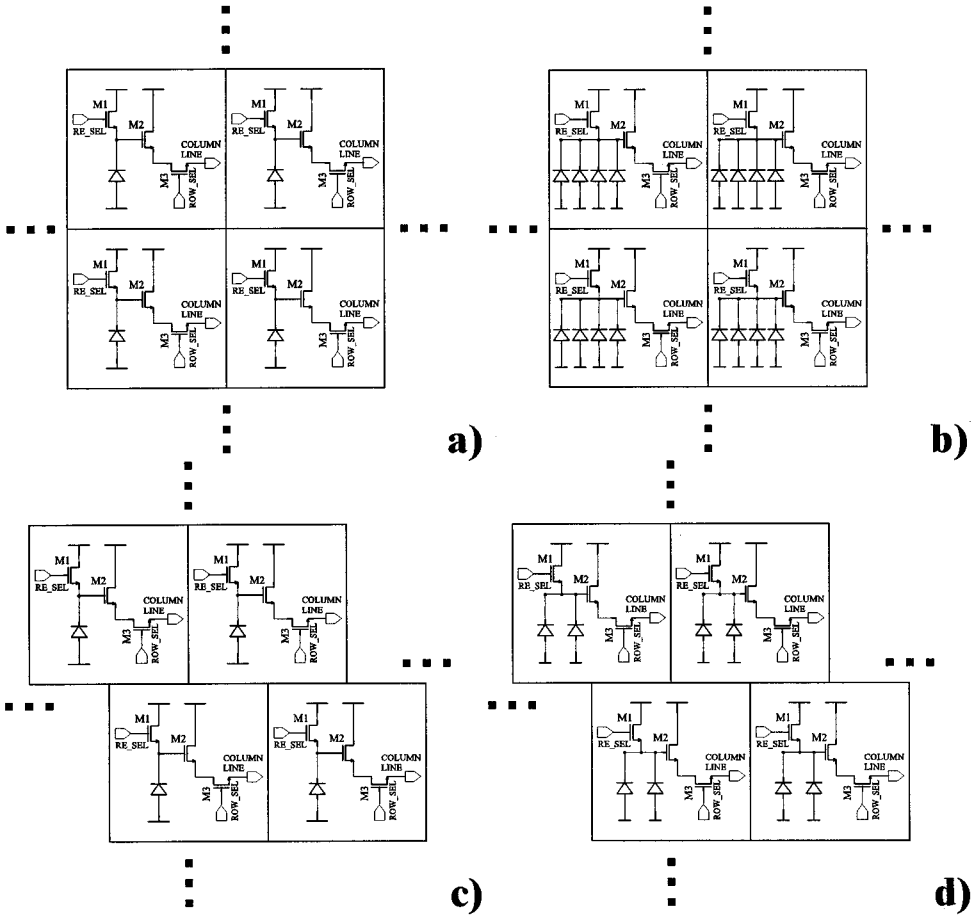



Fig. 2. Main pixel configurations and array layouts in MIMOSA I (a), (b) and in MIMOSA II (a), (c), (d).

with two diodes instead of four diodes was implemented in MIMOSA II.

### C. Noise Performance

The primary sources of pixel readout noise are kTC reset noise and amplifier (from the pixel source follower and the output voltage amplifier) thermal and flicker (1/f) noise. The dark current shot noise becomes important only at higher detector temperatures, while below 0°C it is completely dominated by the other sources of noise. The estimated kTC reset noise is $32e^-$ and $62e^-$ accordingly for the lowest and the highest detector capacitance in Table I. The pixel thermal and flicker noise spectrum density can be estimated by fitting the *SPICE* simulated curves to the following expression:

$$S(f) = S_0\left(1 + \frac{f_c}{f}\right) \tag{3}$$

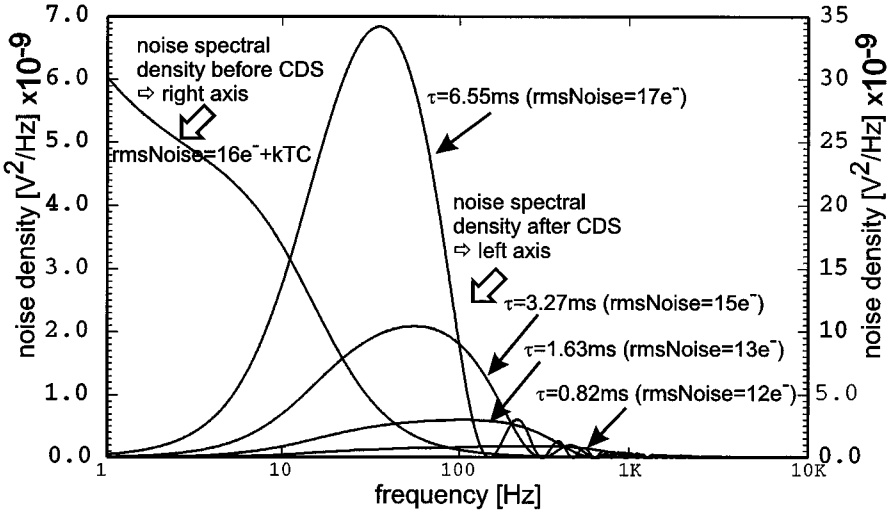
where $S(f)$ is the total spectral noise density referred to the input, $S_0$ is the fitting component and $f_c$ is the flicker noise corner frequency. In order to remove the kTC noise, the CDS signal processing technique was used with the temporary noise sampled twice after the pixel reset. The CDS processing suppresses the low frequency noise components, at the expense of increased thermal noise contributions. The noise spectral density after CDS is given by the following formula:

$$S_{\text{out}}(f) = 4\left[\frac{\sin(\pi f \tau_{\text{int}})}{\pi f \tau_{\text{int}}}\right]^2 \times \sum_{n=0}^{\infty}\left[S_{\text{in}}\left(f - \frac{n}{\tau_{\text{int}}}\right) \times \left[\sin(\pi f \tau_{\text{int}})\right]^2\right] \tag{4}$$

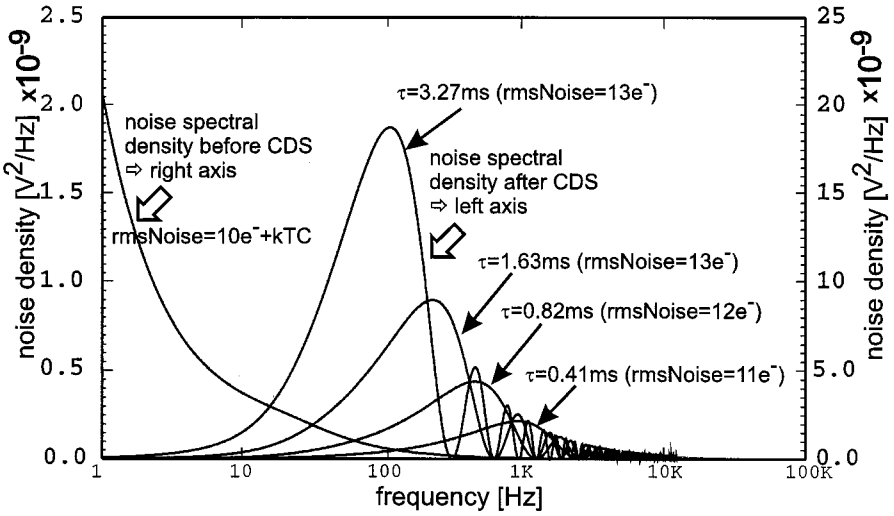
TABLE I
ESTIMATED ELECTRICAL PARAMETERS OF MIMOSA CHIPS

| MIMOSA I | 1 diode | 4 diodes |
|---|---|---|
| total node capacitance @ 3.2 V | 10.9 fF | 26.2 fF |
| diode capacitance @ 3.2 V | 3.1 fF | 4x3.1 fF |
| conversion factor (after SF*) | 13.9 μV/e⁻ | 5.8 μV/e⁻ |
| diode leakage current @ 27°C | 5 fA | 4x5 fA |
| noise (CDS 1.25 MHz) | 15 e⁻ | 32 e⁻ |

| MIMOSA II | 1 diode n-radtol. | 1 diode radtol. | 2 diodes radtol. |
|---|---|---|---|
| total node capacitance @2.5 V | 6.2 fF | 7.1 fF | 9.4 fF |
| diode capacitance @ 2.5 V | 1.65 fF | 1.65 fF | 2x1.65 fF |
| conversion factor (after SF*) | 25.7 μV/e⁻ | 22.6μV/e⁻ | 16.9 μV/e⁻ |
| diode leakage current @ 27°C | 0.25 fA | 0.25 fA | 2x0.25 fA |
| noise (CDS 2.5 MHz) | 11 e⁻ | 13 e⁻ | 17 e⁻ |




(a)




(b)

Fig. 3. Output noise spectral densities before (right $y$ axis) and after (left $y$ axis) CDS processing for MIMOSA I (a) and MIMOSA II (b) as a function of different CDS intervals equal to signal integration time values. The presented ENC values were obtained by a numerical integration of power spectral densities.

where $S_{\text{in}}(f)$ is the output noise power spectral density before CDS processing. It is a product of the pixel noise spectrum density at the input of the readout amplifier and its transfer function $H_{\text{amp}}(f)$, that can be expressed by

$$S_{\text{in}}(f) = S(f) \times |H_{\text{amp}}(f)|^2 . \tag{5}$$

The r.m.s. value of the noise expressed in equivalent number of electrons (ENC) depends on the DC voltage gain $G_v$ of the readout amplifier and on the charge-to-voltage conversion gain of the pixel $G_C$. It is then calculated by

$$(\text{rmsNoise})^2 = \frac{\int_0^\infty S_{\text{out}}(f)\, df}{G_v G_C q} \tag{6}$$

where $q$ is the elementary electronic charge. Fig. 3 shows the noise power spectral densities for both MIMOSA chips, where sampling frequencies of 0.625, 1.25, 2.5, 5, and 10 MHz were examined. For the sake of later measurements, only the four lowest (four highest) sampling frequencies were considered in the case of MIMOSA I (MIMOSA II). The ENC values of the noise presented in this figure were obtained by a numerical integration of power spectral density distributions.

The radiation tolerant design demands a compromise with respect to noise optimization, since the dimensions of the transistors cannot be chosen freely. The standard nonradiation tolerant design gives an ENC 10 to 20% better than the design with all transistors enclosed. The noise bandwidth of MIMOSA II, because of the increased speed of the output amplifier, is wider than the one of the predecessor and thereby the noise behavior could potentially be worse. Thus, the pixel source follower was loaded in MIMOSA II with an additional capacitance $C = 2.5$ pF, decreasing the ENC by 10% with regard to the initial value. The r.m.s. value of the noise after CDS processing of the output amplifier referred to its input was estimated to be 46 $\mu$V and 72 $\mu$V for MIMOSA I and II, respectively.

The main parameters of both prototypes are summarized in Table I. The presented numbers were obtained doing analytical

calculations and post-layout simulations with the *spectreS* circuit simulator.

## III. Charge Collection Simulations

The charge collection efficiency of the MAPS device was verified using the ISE-TCAD package [8]. The device geometry, as described by a mesh generated by the MESH-ISE program using the boundary definition and doping information was examined by DESSIS-ISE, a multidimensional, mixed-mode device and circuit simulator. The mesh was generated using the analytical description of doping profiles inside the detector. This doping information was based on the real twin-tub CMOS fabrication process.

In the computations that were carried out, DESSIS-ISE was used to solve the semiconductor device equations for the drift-diffusion carrier transport model in three dimensions. The *alpha-particle* model, available for transient simulations, was used to describe an excess charge due to a single passage of an ionizing particle. A uniform charge distribution along the particle track with a value of 80 eh/$\mu$m was assumed. The radial charge distribution was declared gaussian with a width $\sigma = 0.75$ $\mu$m. The maximum simulated volume of the detector was $122 \times 122 \times 40$ $\mu$m$^3$, filled with a generated mesh of up to 125 000 vertices. The thickness of the simulated structure was varied according to the considered thickness of the epitaxial layer. The highly doped substrate was described by a constant thickness of 15 $\mu$m for all analyzes. Using a thicker substrate layer is of no significance for the collected charge, since the substrate contribution is shown to be limited to the first 10 $\mu$m of its depth [9]. The whole simulated structure, comprising nine adjacent pixels, was prepared in a way allowing overcoming limitations of the reflective boundary conditions (a default option in DESSIS-ISE) and to keep the simulation time as short as possible. Pixels were laid down with a pitch of 20 $\mu$m in a square array of 3-by-3 elements.

The drift-diffusion model, used to study the charge collection mechanism, is based on three equations, i.e., the Poisson equation and two continuity equations for electrons and holes. The specific design of the detector prevents the holes from giving a significant contribution to the total collected charge. In addition, the density of the charge created in any part of the detector at room temperature is negligible compared to the density of the ionised atoms of impurities. The last feature simplifies the right-hand side of the Poisson equation, given by

$$\varepsilon \nabla^2 \Psi = -q\left(p - n + N_D^+ - N_A^-\right) \tag{7}$$

where $\varepsilon$ is the electric permitivity, $\Psi$ is the electrostatic potential, $q$ is the elementary electronic charge, $n$ and $p$ are the electron and holes densities and $N_D^+$ and $N_A^-$ are the densities of ionised donors and acceptors. The (7) depends now only on the densities of ionised donors and acceptors. Because the density of the generated excess charge is negligible compared to the densities of the ionised impurities the distribution of the electric field does not depend on it, justifying the use of the steady state solution for the electrostatic potential during the transient analysis. Taking into account the aforementioned arguments, the transient charge transport mechanism was analyzed by solving only the continuity equation for electrons. The collected charge was obtained by a straightforward integration of transient currents on the collecting diode contacts. The potential of contact nodes remained constant and contact electrodes were biased from the 3-V voltage source.

TABLE II
Geometrical Simulation Parameters

| | |
|---|---|
| single pixel size | x=20 μm, y=20 μm |
| number of diodes per pixel | one |
| diode size | 3x3x3.2 μm$^3$ |
| diode position | centre pixel |
| substrate thickness | 15 μm |
| epitaxial layer thickness | 5 μm, 15 μm, 25 μm |
| simulated structure size | 3-by-3 pixels |

An appropriate set of dependencies and physics models including all important parameters for the charge collection mechanism was chosen. The doping dependent mobility of the charge carriers was modeled according to Masetti *et al.* [8]. For all the simulations, a uniform device temperature of $T = 300$ K was assumed and the high field saturation model according to Canali *et al.* [8] was chosen. For the net recombination rate, required for the drift diffusion model, only the contribution due to Schockley–Read–Hall (SRH) mechanisms was taken into account. The minority SRH carrier lifetimes, from the doping concentration, were determined by the Scharfetter relation [8]. As necessary parameters for the latter model, the default values for silicon were used. The doping dependent electron lifetimes were estimated to 10 ns, 10 $\mu$s and about 1 $\mu$s in the substrate, in the epitaxial layer and in the $p$-well, respectively. The carrier lifetime is a crucial parameter for the charge collection in the MAPS device. The very short carrier lifetime in the substrate, combined with the degraded mobility due to the high doping level, limits the charge spreading possibility in this region. This fact reduces the substrate contribution to the total collected charge.

The active volume of the detector is the epitaxial layer, since most of the collected charge originates in it. The thickness of this layer, which is a characteristic feature for a given fabrication process, was used as a parameter. Simulations were performed for three different values of 5 $\mu$m, 15 $\mu$m, and 25 $\mu$m. The main geometrical parameters of the simulated structures are summarized in Table II. These parameters define the detector geometry, which corresponds roughly to both MIMOSA chips architectures and the hypothetical design with thick epitaxial layer.

For each thickness of the epitaxial layer, 33 separate analyzes, each devoted to a single event at fixed impact point of the ionizing particle, were performed. Two characteristic parameters, i.e., the charge collection efficiency and the collection time, were determined for each point. The impact positions were chosen randomly using the *design-of-experiment* (DOE) option available when running the GENESIS-ISE environment. The charge collection efficiency and the collection time were analyzed for three different cluster configurations depending on the distance between the impact position and the centre of the collecting diode in the central pixel. The results, presented in Fig. 4, show the charge collection efficiency (expressed as the number of collected electrons) and the collection time for three

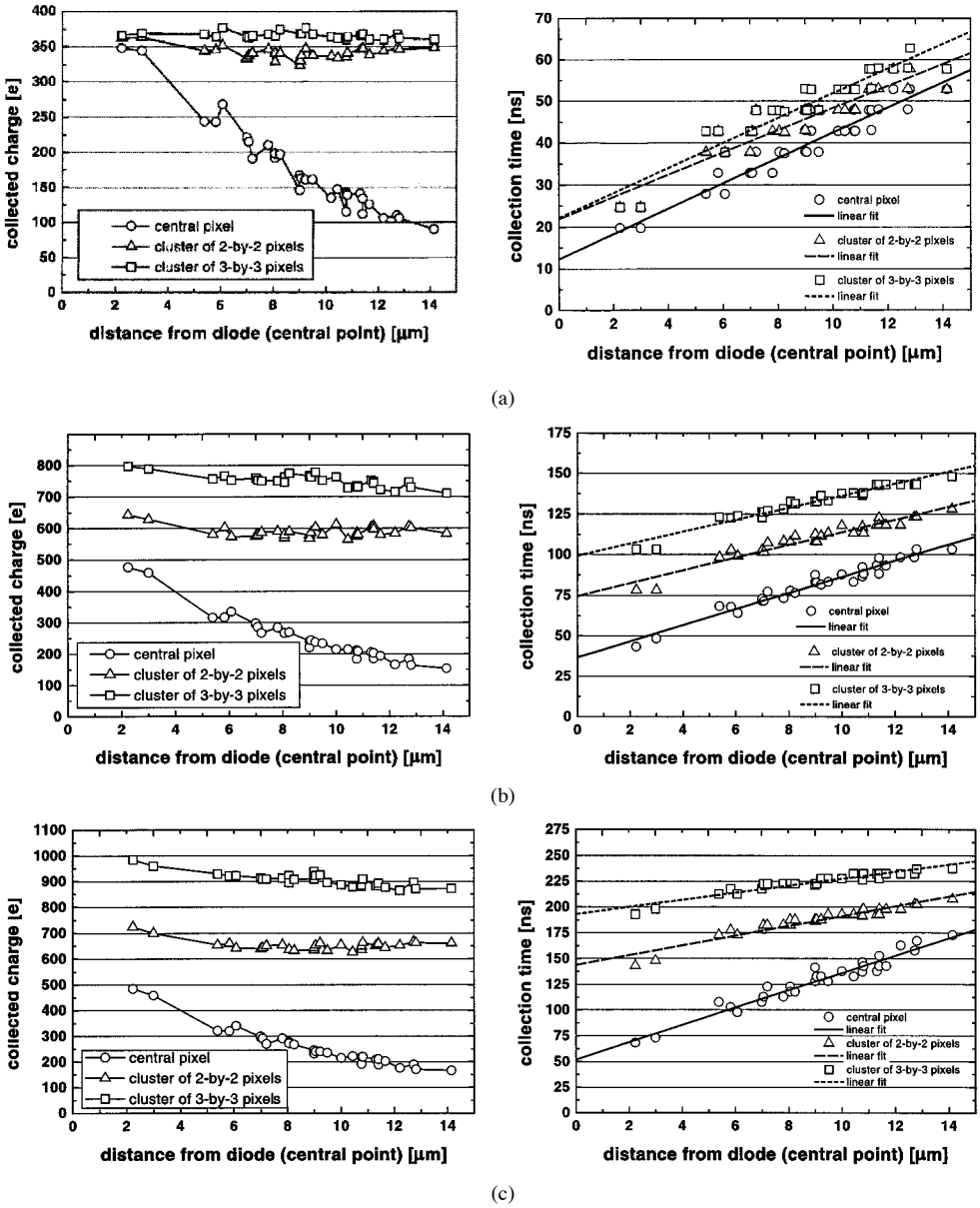



Fig. 4. Simulated charge collection efficiency (expressed as the number of collected electrons) and collection time as a function of the distance between the impact position and the centre of the pixel for (a) 5 $\mu$m, (b) 15 $\mu$m, and (c) 25 $\mu$m thick epitaxial layers.

values of the epitaxial layer thickness versus the distance between the particle impact point and the diode position within the pixel.

Three cluster definitions were considered, comprising either only the central pixel, or the four pixels exhibiting the highest signals, or all nine pixels closest to the impact position. Fig. 4 shows that the charge spreading among neighboring pixels increases with the epitaxial layer thickness. For a thickness of 5 $\mu$m nearly all the collected charge is located in a cluster of 2-by-2 pixels. The charge collected on the central pixel depends strongly on the hit position: it is minimal when the impact position is at equal distance from the four closest pixel centres (corner hit), regardless the epitaxial layer thickness. The charge collected in this case is less than a quarter of the total charge found in a cluster of 3-by-3 pixels. The charge collected on the central pixel first increases with increasing thickness of the epitaxial layer and then starts saturating when the epitaxial layer thickness gets comparable to the pixel pitch. The growth of the collected charge with the epitaxial layer thickness is weaker for the central pixel than for clusters of $2\times2$ or $3\times3$ pixels. The collection time, which is defined as the time after which 90% of the total charge is collected, increases as well with the epitaxial layer thickness and depends also on the impact position: the shortest collection time is observed for the central hit, i.e., when the impinging particle passes through the collecting diode. In this case nearly all the available charge is collected on the central pixel. The longest collection time occurs for corner hits and intermediate cases exhibit a nearly linear dependence on the hit distances from the middle point of the central pixel.

## IV. Experimental Results

Both the MIMOSA I and MIMOSA II chips were extensively tested with ionizing radiation. All tests were performed with

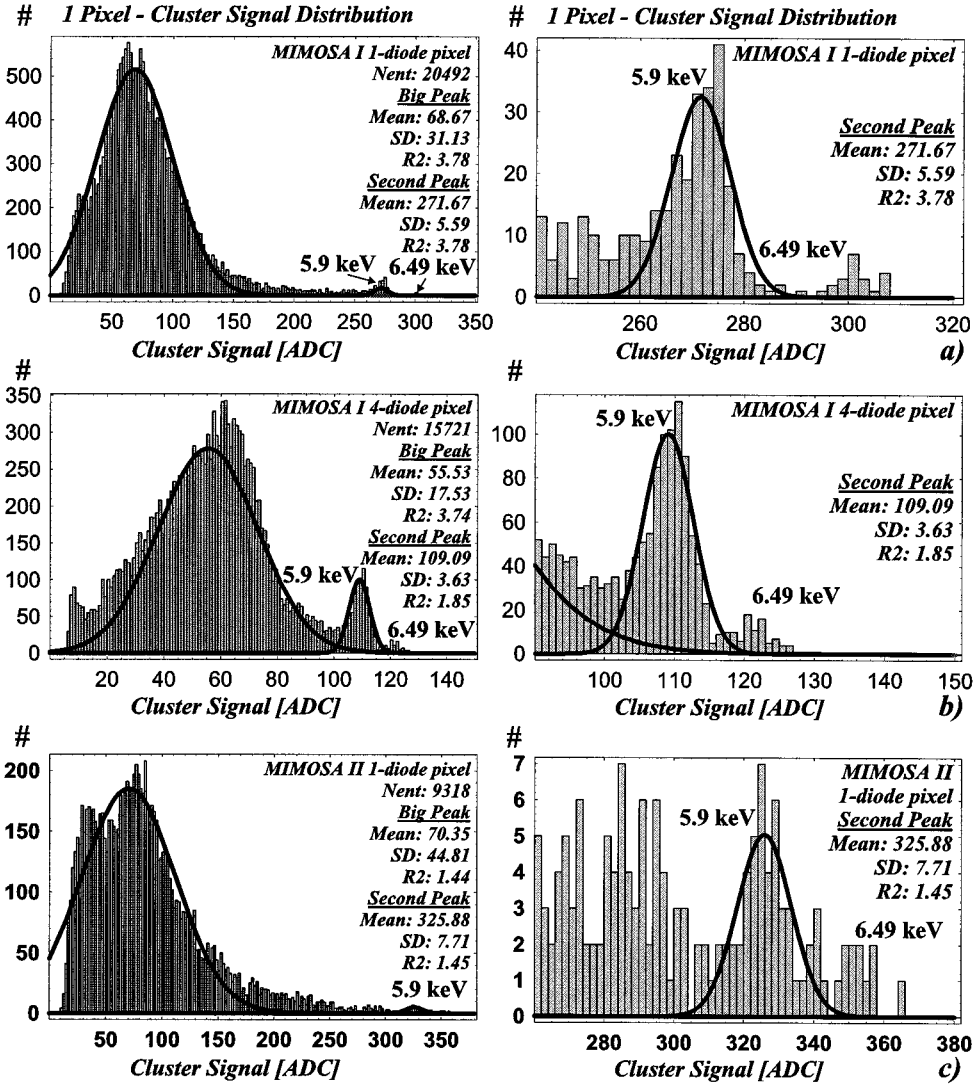



Fig. 5. Signal pulse height distribution for photons emitted by an $^{55}$Fe source measured on the central pixel in the clusters observed with the MIMOSA I sensor in the case of 1 and 4 diodes per pixel, and the MIMOSA II chip in the case of 1 diode per pixel. The histograms to the right show the peak, which is taken as reflecting 100% collection efficiency originating from the photons, converted near the diodes.

the specific data acquisition system based on an OS9 processor. The individual pixels were addressed in consecutive clock cycles and an external 12-bit ADC unit was used to digitise the raw analogue signals. Data from two consecutive frames (8092 samples) were kept in a circular buffer memory. The acquisition was stopped after trigger (particle) arrival, with a delay corresponding to the readout time of one frame. This approach defined the charge integration time equal to the readout time of the whole frame, although the sampling frequency of the ADC used was 4096 times higher. The CDS signal processing was performed by calculating a difference between the data in two consecutive frames, i.e., before and after the trigger arrival. After CDS, the signal generated by the particle interaction could easily be extracted, being only superimposed on a fixed voltage offset (pedestal) from the leakage current. Most of the MIMOSA I prototype measurements were done at a temperature near $-10\,^{\circ}$C (beam tests), using 1.25 and 2.5-MHz readout clock frequencies. The major motivation for cooling was to increase the time interval between consecutive reset cycles. The diode leakage current modifies the voltage of the charge-collecting node and if the leakage current is too high, this voltage (still amplified on the chip) moves rapidly out of the dynamic range of the ADC. The cooling reduced the leakage current and the reset cycle could be slowed down to a few hertz only. The cooling is not important for the shot noise due to the leakage current, because this contribution is negligible for practical frame rates, compared to other noise sources. The cooling is important for convenience of the beam tests, where the triggers are randomly distributed in time and not synchronised with the pixel resetting. In the case of MIMOSA II, a higher readout frequency was used (10 MHz) and since the diode reverse current was an order of magnitude lower due to the different fabrication process (Table I), most of the measurements were performed at room temperature.

### *A. Device Calibration Using Soft X-Rays*

The major goal of the calibration performed with a $^{55}$Fe 5.9 keV photon source was to measure the conversion gain, which is

TABLE III
MEASURED ELECTRICAL PARAMETERS OF MIMOSA SENSORS

| MIMOSA I | 1 diode | 4 diodes |
|---|---|---|
| conversion factor (after ADC) | 6.1 $e^-$/ADC | 14.9 $e^-$/ADC |
| conversion factor (after SF) | 14.6 μV/$e^-$ | 6.0 μV/$e^-$ |
| total node capacitance @ $V_{DD}$=5V | 10.9 fF | 26.6 fF |
| noise (CDS 1.25 MHz @ T=-20°C) | 14 $e^-$ | 30 $e^-$ |
| **MIMOSA II** | **1 diode rad-tolerant** | **2 diodes rad-tolerant** |
| conversion factor (after ADC) | 5.1 $e^-$/ADC | 6.7 $e^-$/ADC |
| conversion factor (after SF) | 22.9 μV/$e^-$ | 17.5 μV/$e^-$ |
| total node capacitance @ $V_{DD}$=5V | 7.0 fF | 9.1 fF |
| noise (CDS 2.5MHz @ T=+20°C) | 12 $e^-$ | 14 $e^-$ |

needed for further parameterization, in absolute units, of the device performance. Such photons undergo photoelectric interaction inside the active detector volume. Neglecting other energy losses but ionization, a constant number of charge carriers, i.e., 1640 e/h pairs in silicon is generated. This gives rise to a characteristic peak in the signal amplitude distribution. For detectors having close to 100% charge collection efficiency, the position of this peak can be directly used for measurements of the conversion gain. This is not the case of the present device, where the carrier transport mechanism is dominated by thermal diffusion, leading to only partial charge collection. The charge is naturally spread among several pixels. However, the assumption of fully efficient charge collection is justified for a small subsample of photons converted inside the depleted volume of the collecting diode pn junction. This can explain the presence of the second, smaller peak visible in the central pixel photon spectrum shown in Fig. 5. Thorough analysis shows no charge collected onto the adjacent pixels for events in the second peak. Next, closer examination of the second peak allows distinguishing the next still smaller peak shifted to the right. The ratio of entries numbers in both peaks as well as peaks mutual positions allow identifying two emissions modes from the $^{55}$Fe source. These facts justify previous statement on fully efficient charge collection for some events and the position of this particular peak for 5.9-keV photons was used to measure the conversion gain and consequently other basic electrical parameters. The obtained data is summarized in Table III.

### *B. Properties of the Signal Generated by Minimum Ionizing Particles*

The response of the MIMOSA chips to minimum ionizing particles (MIP) traversing a CMOS sensor was studied using a 120 GeV/c pion beam from the CERN SPS accelerator. For these tests, pixel detectors were mounted inside a high precision beam telescope [10]. A small scintillation counter adapted to match the physical dimension of the tested device was delivering a trigger.

Both MIMOSA prototypes were successfully tested. This paper gives a detailed overview of the data analysis results and conclusions for MIMOSA I. The MIMOSA II data analysis being still under way, only some of its (preliminary) results are shown.

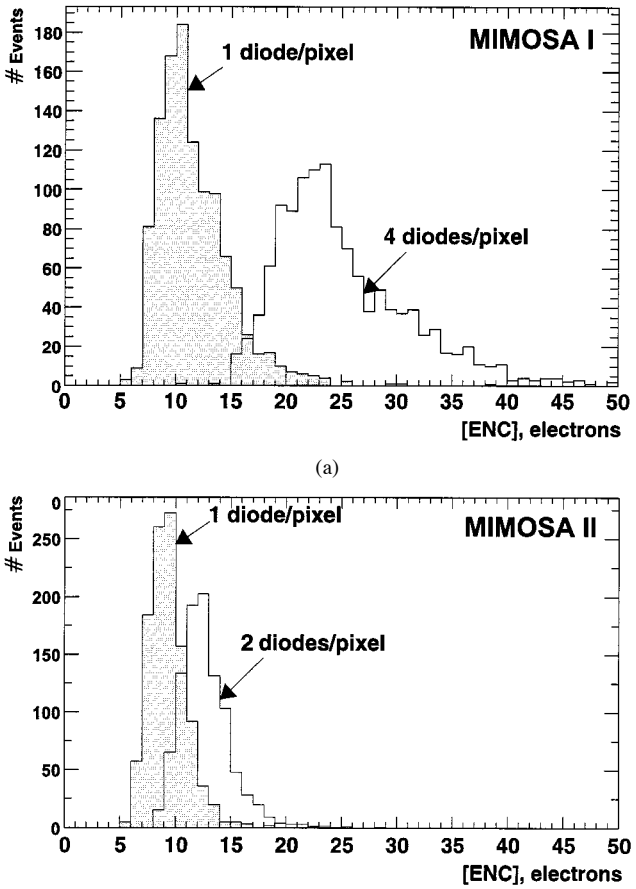



Fig. 6. Individual pixel noise distributions for MIMOSA I (a) and MIMOSA II (b) for different implemented pixel configurations.

The full description of the beam test set-up and the methodology of the data analysis can be found elsewhere [11]. The distribution of the individual pixel noise, defined as a fluctuation of the signal (after CDS processing) around its pedestal value, is shown in Fig. 6. The mean ENC was found to be equal to 12 and 25 electrons for the 1- and 4-diode pixel configurations in MIMOSA I, respectively and accordingly 9 and 13 electrons for the 1- and 2-diode configurations of MIMOSA II. Overall values agree well with prior calculations and measurements, despite the small discrepancies between the noise values shown in Table III and those of Fig. 6, which are likely originate from different test setup arrangements and the way in which data was acquired.

Fig. 7 displays the signal-to-noise ratio for the central pixel of a cluster for minimum ionizing particles for MIMOSA I. The central pixel was identified by requesting an individual signal to noise ratio above five and taking the pixel with the highest signal value within a cluster of neighboring pixels. The variation of the collected charge as a function of the cluster size is plotted in Fig. 8 for both prototypes. Pixels were successively added to the cluster in decreasing order of their signal amplitudes. The charge spread appears to be limited to about 16 pixels per cluster for both pixel configurations in MIMOSA I and about 12 for MIMOSA II. The absolute amount of the collected charge is about 20% larger for the 4-diode design in MIMOSA I and 10% higher for the 2-diode design in the second chip. The variation of the clusters signal-to-noise ratio with their size (Fig. 9) exhibits

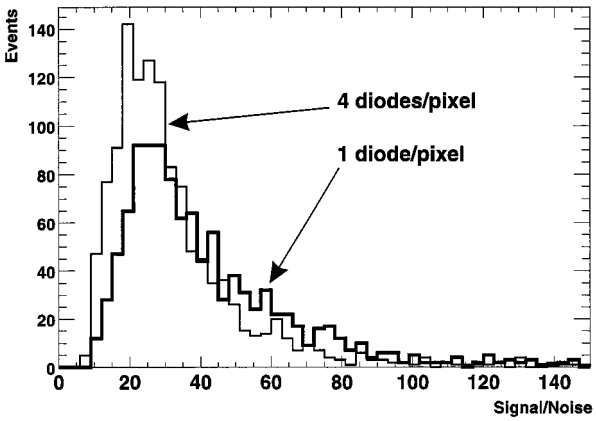



Fig. 7. Signal-to-noise distribution for the cluster central pixel.

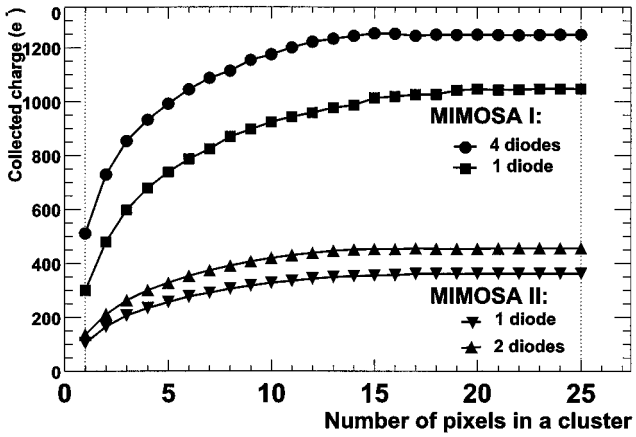



Fig. 8. Collected charge (most probable value) as a function of the cluster size.

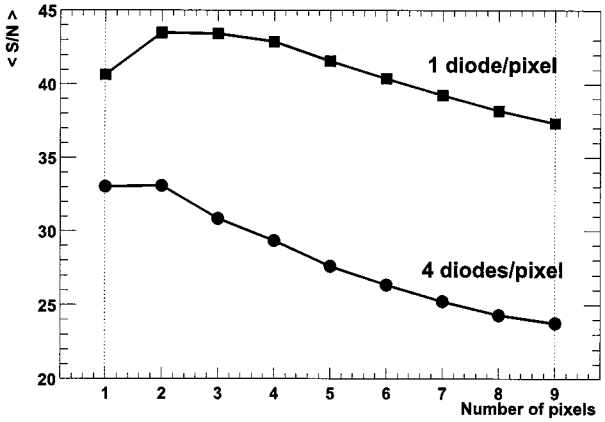



Fig. 9. Signal-to-noise (mean value) as a function of the cluster size.

better performances for one diode per pixel. The mean value of the signal-to-noise ratio reaches 43 in this case. The cluster noise was taken here as the average single-pixel noise times the square root of the cluster multiplicity.

### *C. Tracking Performance of the MIMOSA I Prototype*

In order to determine the pixel detector spatial resolution, the track parameters extracted from the reference beam telescope were compared to the position extracted from the pixel device using two different methods. In the first method (digital resolution), the track position is given by the centre of the pixel exhibiting the highest signal-to-noise ratio in the cluster. In the second method (CoG), the track position is taken as the centre of gravity of the charge within a $3 \times 3$ pixel cluster. Using the second method for 1-diode configuration in MIMOSA I, a gaussian fit to the residuals exhibited a standard deviation of 2.2 $\mu$m. This result could still be improved using a nonlinear

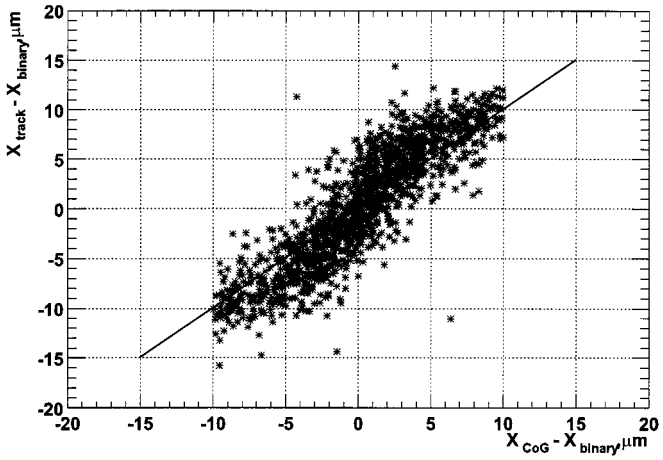
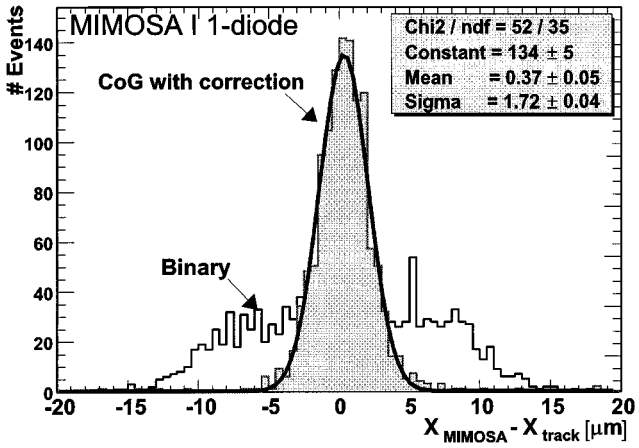
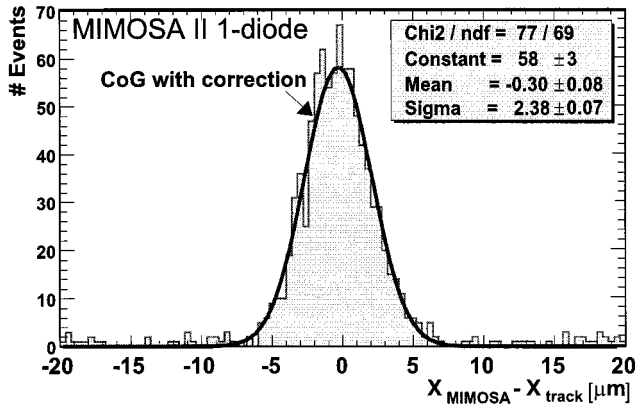



Fig. 10. Correlation between the track positions given by the reference telescope and given by the pixel sensor data using the centre of gravity of a $3 \times 3$ pixel cluster for 1-diode configuration in MIMOSA I.




(a)




(b)

Fig. 11. Residual distribution of a track position measured by the 1-diode pixel in the MIMOSA I sensor using two different algorithms, i.e., binary and center of gravity with the nonlinear correction (a) related distribution for the 1-diode pixel in the MIMOSA II chip using the latter algorithm (b).

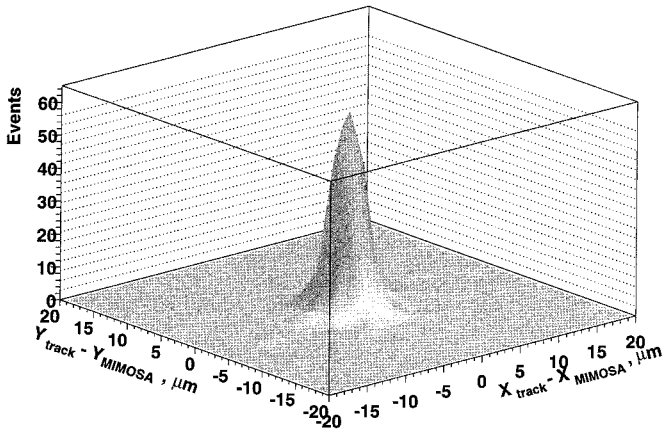



Fig. 12. 2-D distribution of position of all reconstructed clusters with the respect to the reference tracks.

correction to the CoG algorithm. The s-shaped correction function was derived from the correlation between the track position given by the reference telescope and one given by the pixel sensor data using the CoG method (Fig. 10).

After this correction the standard deviation of a gaussian fit to the residual was found to be 1.72 $\mu$m (Fig. 11). Taking into account the estimated precision of the telescope (1 $\mu$m), the spatial resolution of the 1-diode pixel configuration from MIMOSA I based on the centre of gravity position determination algorithm was estimated to be $1.4 \pm 0.1$ $\mu$m in both directions. Following the same algorithm for other pixel configurations and the second prototype, the spatial resolution was estimated to 2.1 $\mu$m and 2.2 $\mu$m for 4-diode and 1-diode configurations in MIMOSA I and MIMOSA II, respectively.

Fig. 12 shows the distribution of the distance between the track position at the pixel plane (measured by the reference telescope) and all clusters reconstructed by the MIMOSA I pixel sensor. For most of the tracks, a cluster was found within a distance of 20 $\mu$m. As a consequence, the detection efficiency of the 1-diode pixel sensors was determined to be $99.5 \pm 0.2\%$ and $98.5 \pm 0.3\%$ in MIMOSA I and II, respectively. The $5\sigma$ for a seed cluster signal-to-noise ratio was used in both cases.

## V. Conclusion

Two prototypes of monolithic CMOS sensors for the detection of minimum ionizing particles were designed and fabricated. The beam tests demonstrate that this detection technique works very efficiently and provides excellent tracking parameters. Thanks to the technology used for their fabrication, monolithic CMOS devices are likely to provide a cost-effective solution for high precision tracking systems, combining advantages of CCDs and hybrid pixel detectors. This makes them an attractive candidate for vertex detectors in future particle physics experiments, as well as for other applications requiring charged particle imaging. The next goal of this development is a large area detector module (in the order of ten $cm^2$). Furthermore, possibilities of integrating various readout functions directly on the sensor and thinning down the substrate to the limits set by its mechanical properties will be investigated. A particular issue will be the improvement of the readout speed and the data sparsification on a chip.

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