



3D Sensors - Vertical Integration of Detectors and Electronics

Contents:

- Introduction to three dimensional integration of detectors and readout electronics
- ILC requirements
- Design of a 3D prototype chip
- Production of thinned, 4-side abutable sensors
- SOI-based sensor/readout integration

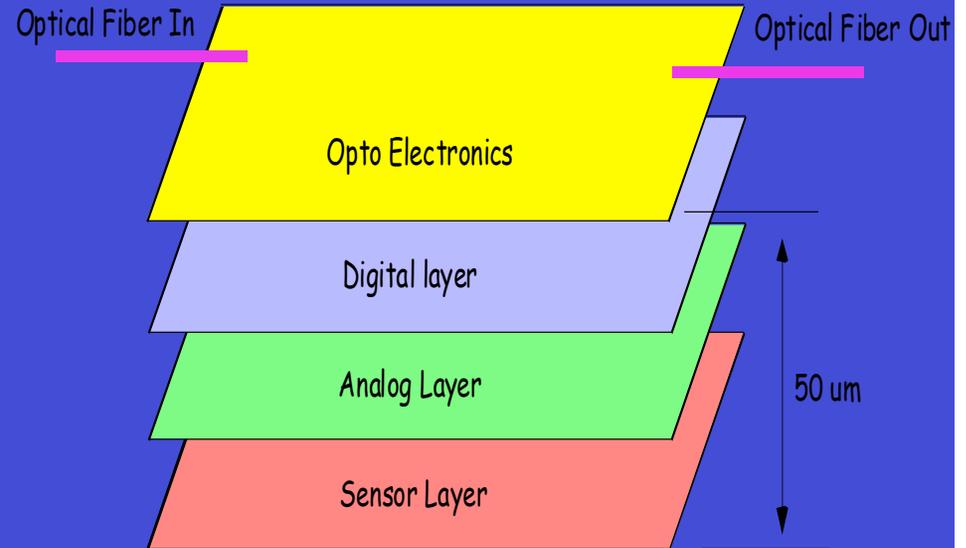
Loose collaboration - Fermilab, Cornell, Purdue, Bergamo

This technology may be new to some - so I will spend some time in explanation.



What is 3D Circuit Integration?

- A 3D chip is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a “monolithic” circuit.
- Frequently, the layers (also called tiers) are comprised of devices made in different technologies.
- The move to 3D is being driven by industry.
 - Going 3D reduces trace length, Reduces R, L, C
 - Improves speed
 - Reduces interconnect power, crosstalk
 - Reduces chip size
 - Processing for each layer can be optimized



Designer's Dream

Key Enabling Technologies

- **Wafer thinning (to $<25\mu\text{m}$)**
 - Grinding, lapping, etching, and chemical polishing
- **Precision alignment**
 - Better than 1 micron
- **Bonding of thinned wafers**
- **Through wafer via formation and metallization**



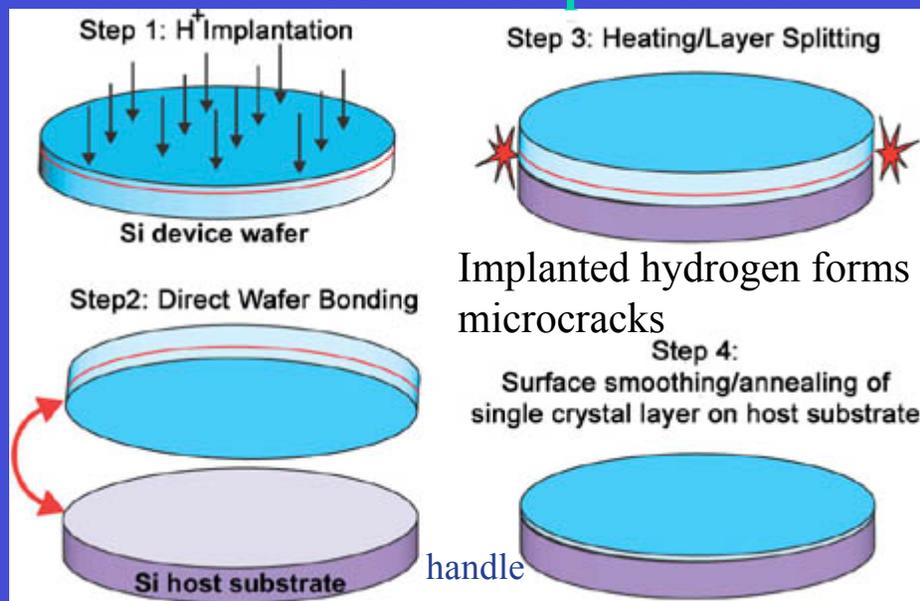
Wafer Bonding and Via Formation

Wafer bonding Technologies

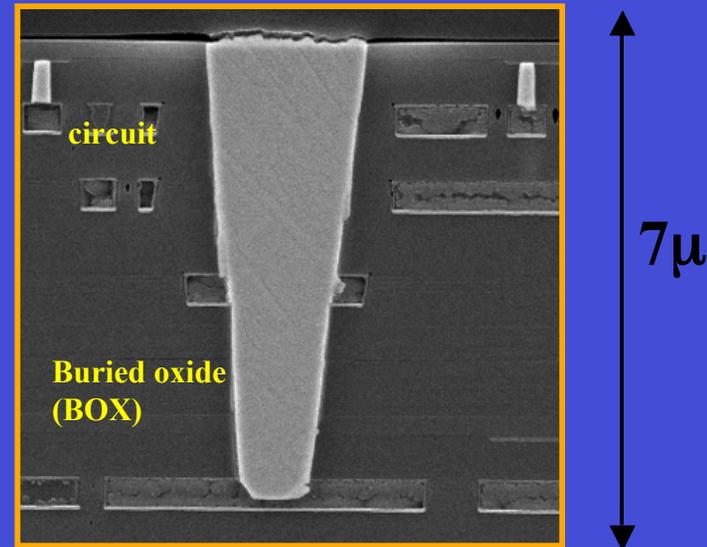
- Direct silicon fusion (used for SOI)
 - Van der Waals initial bond
 - Heating forms covalent bonds
- Cu-Sn eutectic bonding - bumps
- Adhesive bonding (BCP)
- Cu to Cu bonding

Wafer to wafer or die to wafer

“smartcut” SOI wafer production



Via Formation

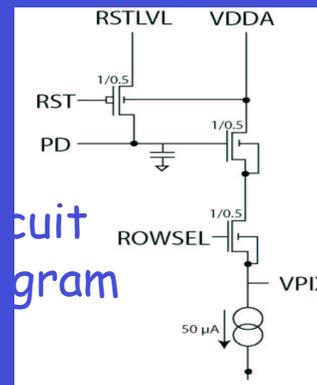
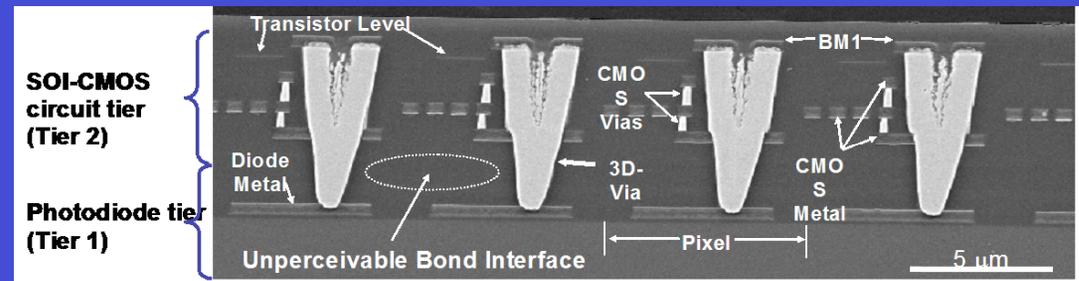


Vias in SOI devices are formed through insulating oxide – do not need special processing for ohmic isolation. Buried oxide also provides an etch stop for thinning. SOI is a preferred technology



Lincoln Labs 3D Image Sensor

- 1024×1024 , $8 \mu\text{m}$ pixels
- 2 tiers
- Wafer to wafer oxide bonding (150 mm to 150 mm)
- $2 \mu\text{m}$ square vias, dry etch, Ti/TiN liner with W plugs
- 100% diode fill factor
- Tier 1 - p+n diodes in $>3000 \text{ ohm-cm}$, n-type sub, $50 \mu\text{m}$ thick
- Tier 2 – $0.35 \mu\text{m}$ SOI CMOS, $7 \mu\text{m}$ thick
- 1 million 3D vias
- Pixel operability $>99.999\%$
- 4 side abutable array



Substantial sharing between ILC and 3D image sensor technology



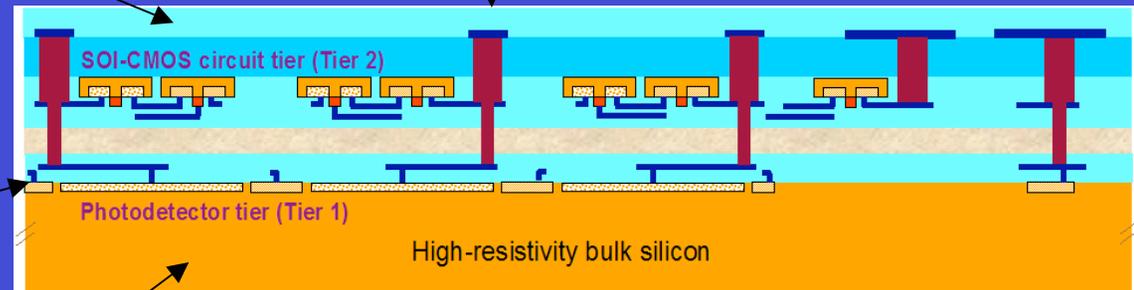
3D Concept for HEP

CMOS circuitry

Interlayer vias

Wafer bond
oxide, intermetallic
or epoxy

7 μm



high resistivity silicon wafer,
Thinned to 50-100 microns

(MIT-LL)

Active edge
processing

Backside implanted after thinning,
before frontside wafer processing

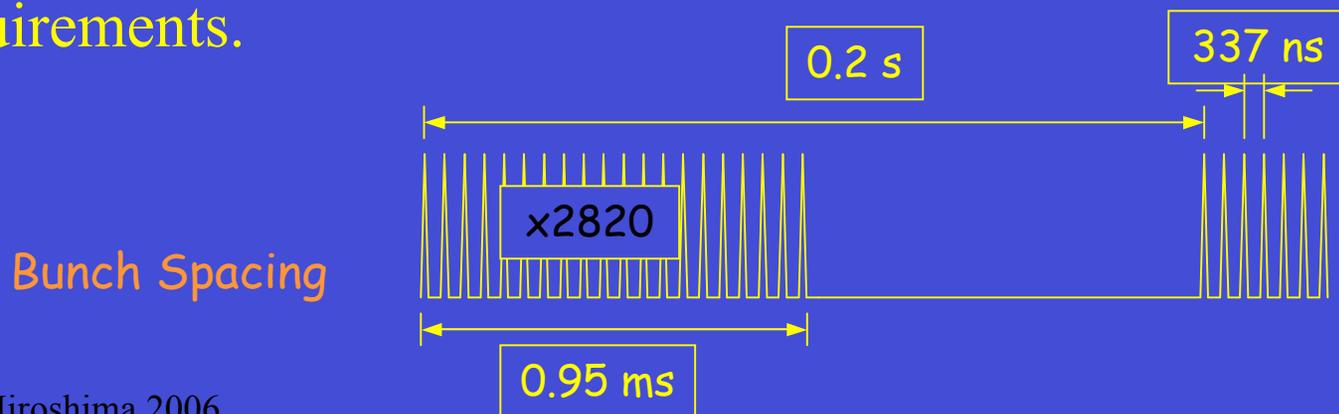


ILC Requirements

The ILC vertex detector is designed for efficient flavor tagging and vertex reconstruction:

- Very low mass - 0.1% r_l per layer
- Resolution < 5 microns in x, y
- Time resolution < 50 microseconds
- Very low power < 20 W (with 1/200 duty factor)
- Inner layer at ~ 1.5 cm radius

The combination of resolution, mass and power is a substantial challenge. None of the candidate technologies (CCDs, DEPFETS, MAPS, SOI) have yet demonstrated a solution which meets all of the requirements.





Advantages of 3D for ILC

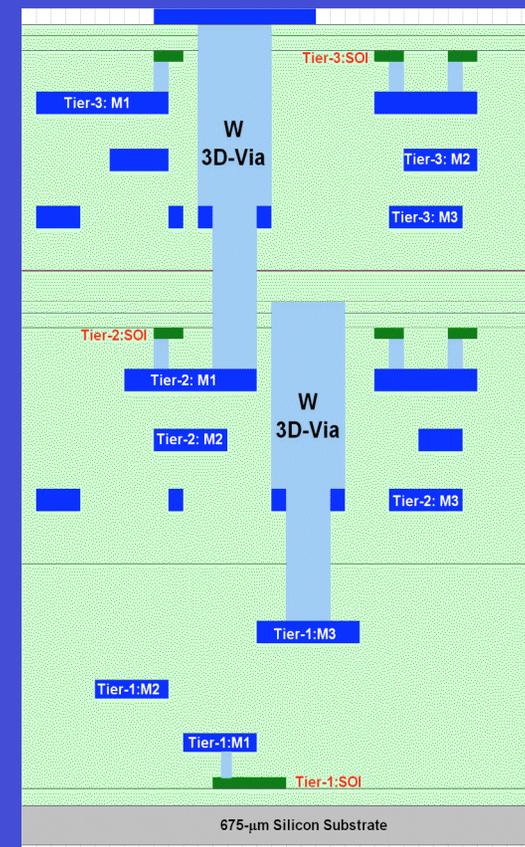
- High resistivity substrate available for fully depleted diodes - large signal
- No limitation on PMOS usage as in CMOS MAPs
- Sense nodes can have *very* low capacitance
- Increased circuit density without going to smaller feature sizes
- Ability to process a field of pixels in upper tiers (reduce transistor count, cluster ...)
- Technologies can be mixed. 3D may be used to add layers above MAPS, CCDS, DEPFETs or other devices under development.
- SOI Radiation hard to >1 Mrad, low SEU sensitivity
- SOI is a low power technology
- Can be made “edgeless”
- Thinning to 50 microns demonstrated
- Minimum charge spreading with fully depleted substrate
- 100% diode fill factor
- “Stitching” traces possible on top tier metal (full wafer mask)



3D Readout for ILC

- Fermilab will contribute an ILC readout chip design to MIT-LL 0.18 micron three tier SOI 3D multiproject run October 1
- ~2.5 mm x 2.5 mm chip, 64x64 20 micron pixels
- Does not include sensor integration
 - Bond readout circuit to an independent sensor wafer (precursor to full 3D integration run)
- Design includes amp/disc, time stamp, pixel control, token passing -
 - Use token passing scheme developed for BTEV pixel and silicon strip RO chips to sparsify data output
 - Do not store pixel addresses in the pixel cell.
 - Store analog and digital time stamps in the hit pixel cell.
 - Store double correlated sample in pixel
- Initial design uses independent pixel cell processing. Multiple cell processing (cell grouping) on multiple tiers will reduce the overall transistor count, but is too complex for the first iteration

(3 transistor levels, 11 metal layers)

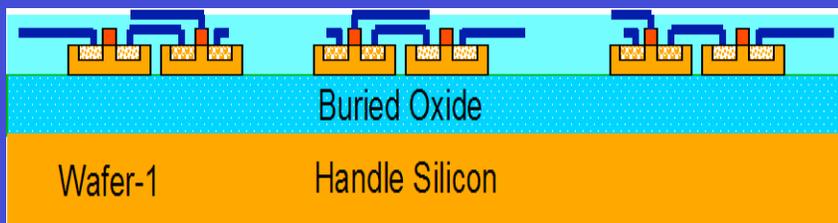
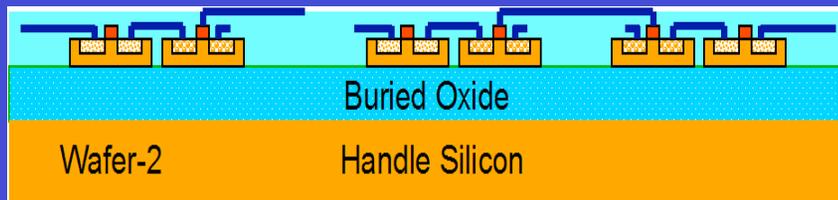




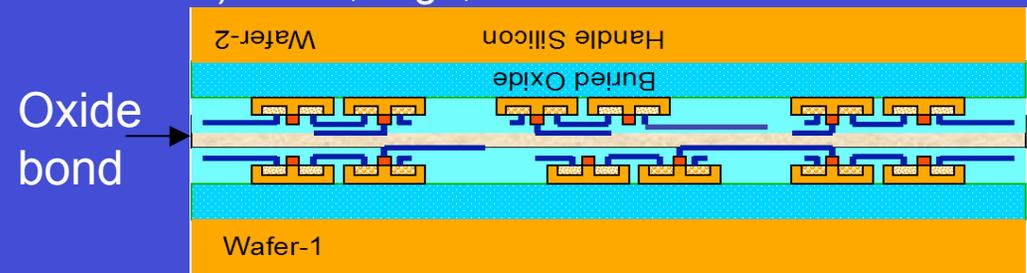
MIT-LL 3D chip

- 3 tier chip (tier 1 RF low Vt transistors)
 - 0.18 μm (all layers)
 - SOI simplifies via formation

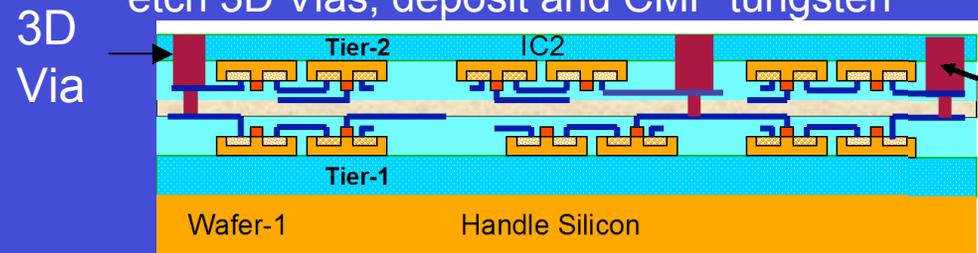
1) Fabricate individual tiers



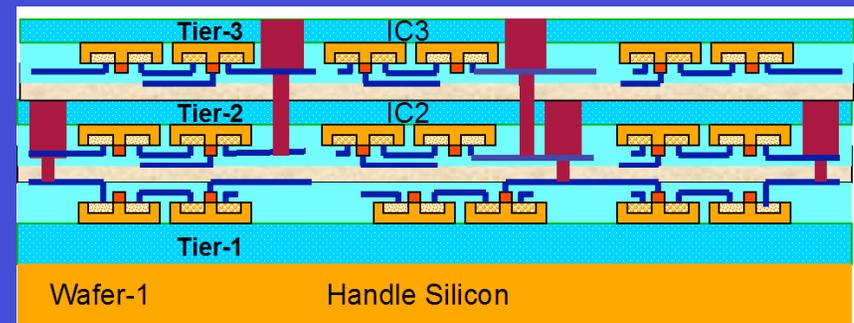
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



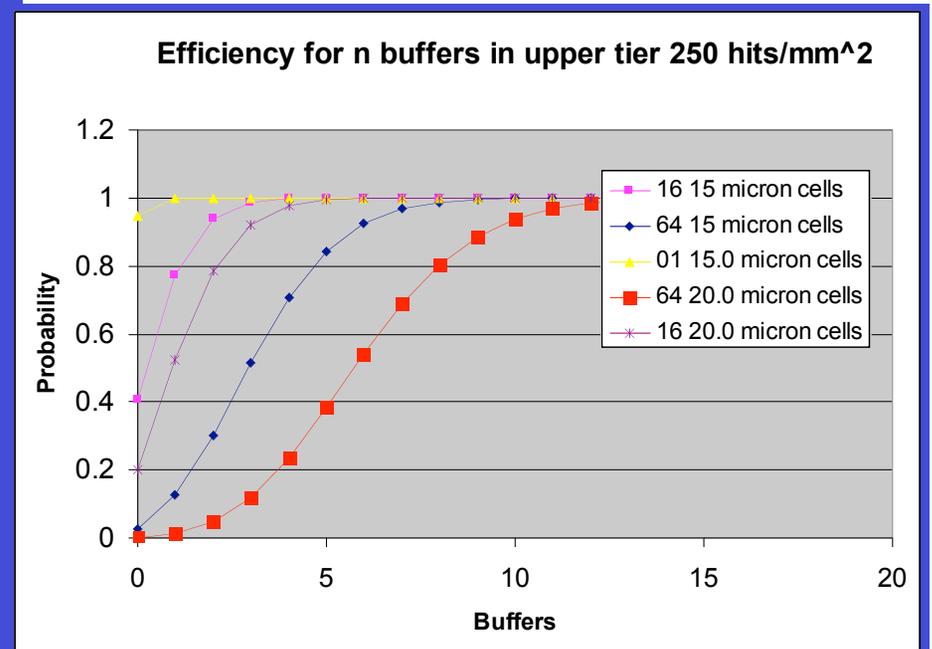
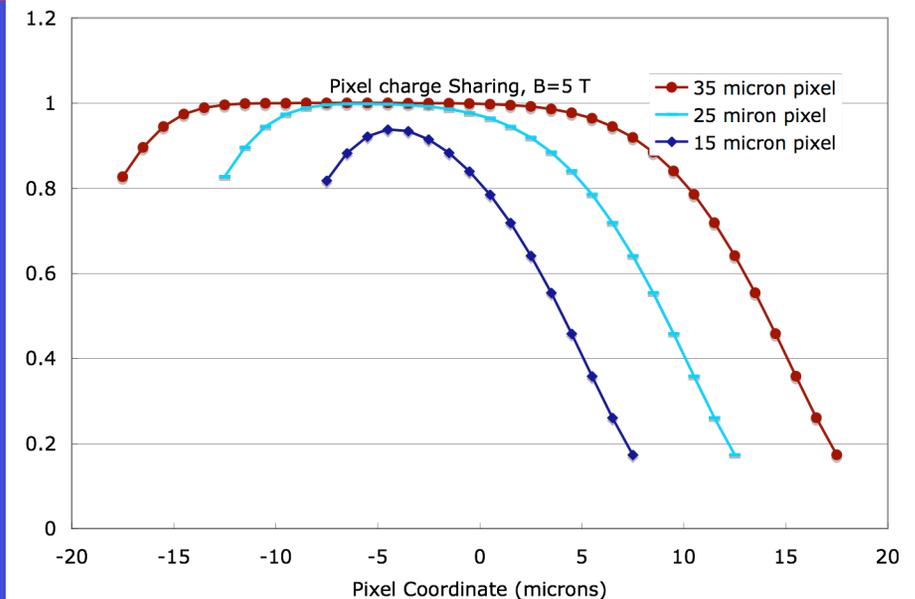
4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3





3D Design Choices

- **ILC Resolution ~ 5 microns**
 - Fully depleted sensors
 - large signal, control of sensor characteristics as “handle wafer”
 - Binary or analog readout? Pixel size
 - Binary implies ~15 micron pixels
 - hard to fit time stamp, test circuit
 - Analog allows larger pixel - but must optimize for charge sharing given B, thickness, signal/noise
- **Time stamp**
 - Resolution set by expected hit density (250/mm² at r~1.5 mm, B=5T) for inner layer pattern recognition
 - Better than 50 microseconds
 - Analog time stamp compatible with analog pixel readout
 - 5 bit digital also fits in pixel (29μs)





Pixel Readout Scheme

- Pixel being read points to the X address and Y address stored on the perimeter
- Outputs the Time Stamp information and pulse height from the pixel.
- While reading out address and time stamp, token scans ahead for next hit pixel (125ps/cell)

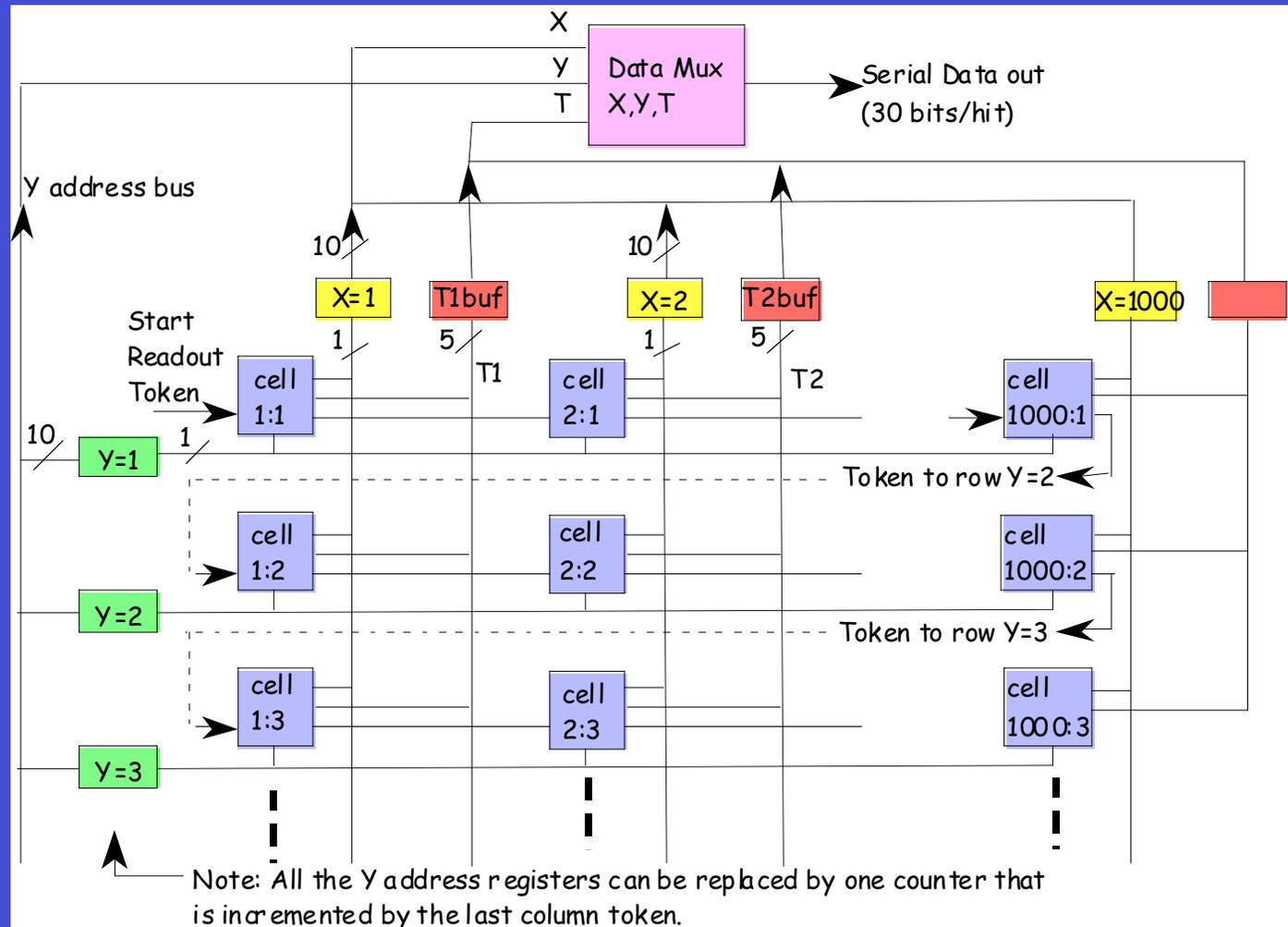
Readout speed:

- 1 Mpixel chip-
- $1000 \times 1000 \times 20 \mu$
- 250 hits/mm²
- 10^5 hits/train

- 20 address bits
- 10 time and q bits

3×10^6 bits/train
20 ns/bit

-> 60 ms (of 199 ms)
Readout can be scaled
by radius to equalize
load





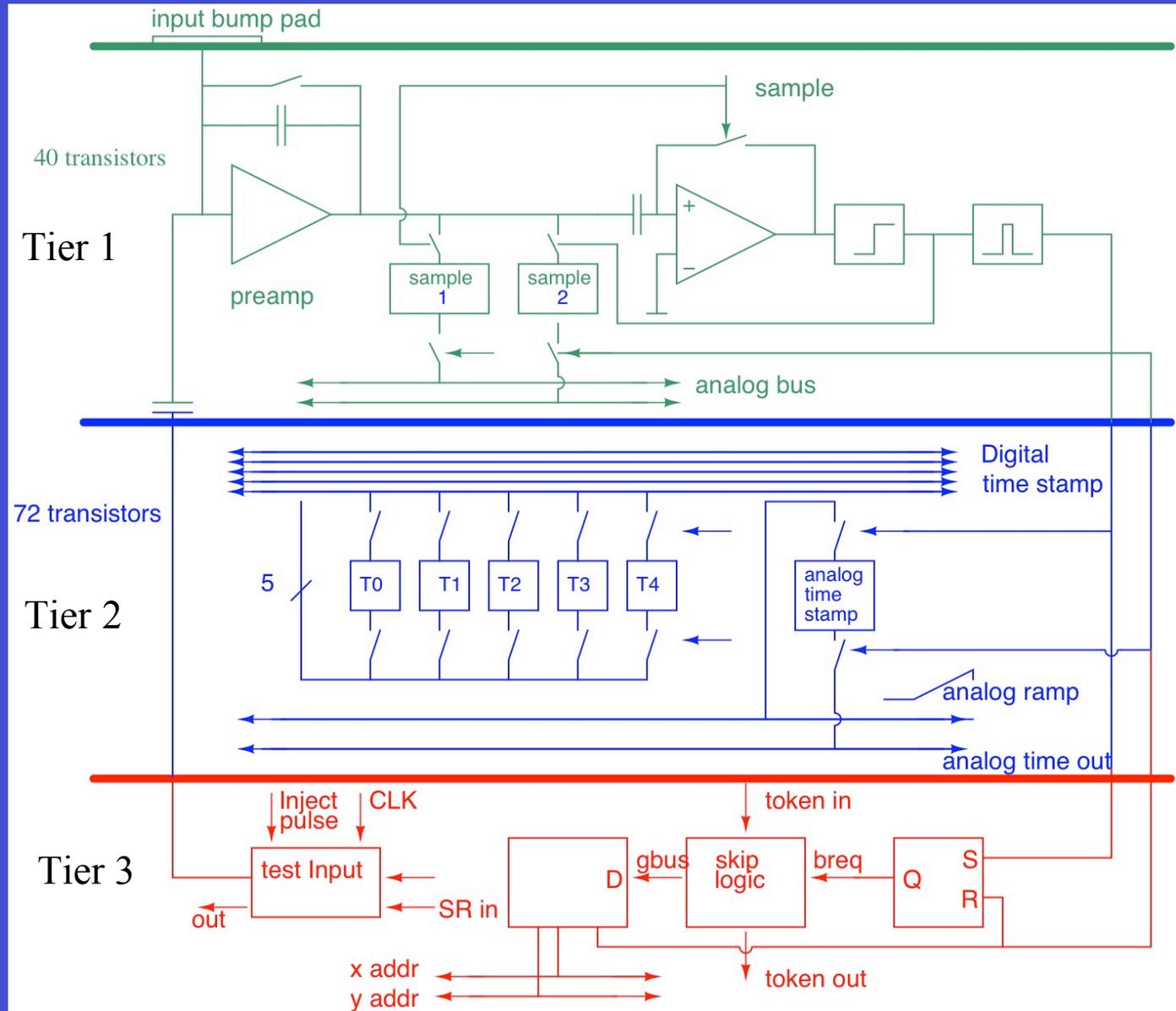
3D Chip design

Correlated double sample
Noise $\sim 35 e^-$ (??)
Adjustable disc. threshold
Few hundred nA/pixel
Most bias currents (times)
adjustable

Analog and digital time
stamps
Analog resolution (?)

Sparse readout
Individual kill/inject

3 vias / pixel





Digital Tier

Virtuoso® Layout Editing: Fermi3D_TierC Sparsifier layoutUp

X: 20.925 Y: 11.825 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 12

Tools Design Window Create Edit Verify Connectivity Options Routing Assura NCSU 3DIC Help

mouse L: showClickInfo() M: leHiMousePopUp() R: leHiEditDisplayOptions()



Sensor R&D

Work on optical imaging arrays is providing technology which is relevant to HEP and ILC vertex detection.

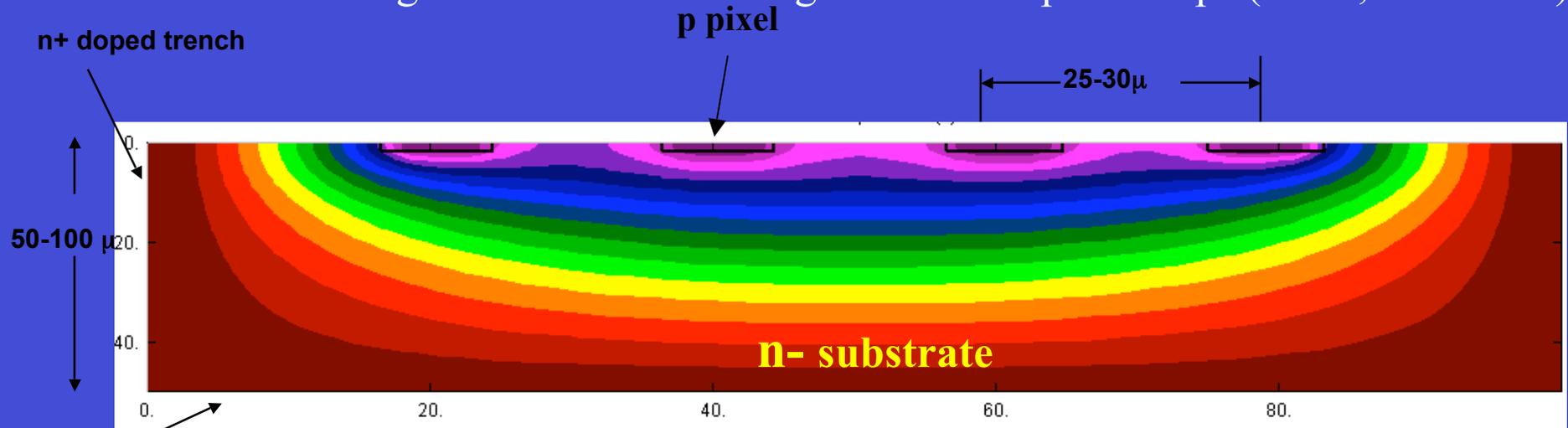
- Fully depleted, thick CCD arrays needed to provide high efficiency infrared detection.
- Techniques for annealing backside doping after thinning to avoid high temperature processing which can damage frontside circuitry. Wafer bonding can be used to include pre-backside processed wafers in a 3D stack.
- Use of deep trench etching to provide defect free edges which can be used as an electrode – eliminating lost space at the edges.

In parallel with the 3D chip design we are fabricating sensor wafers with mating sensors. To be bonded to 3D chips.

Sensor R&D II

- Sensor wafers to be fabricated at MIT-LL, designed at FNAL
 - 6" high resistivity float zone n-type wafers
 - Thinned to 50, 75, 100 microns, implanted + laser annealed (or pre-implanted)
 - 4-side abutable ~no dead space
 - Deep trench etch, n doped polysilicon fill provides edge doping
 - Design variants to minimize noise, avoid breakdown
 - Pinned diode
 - channel stops
 - Geometrical variations
 - Include designs to mate to current generation of pixel chips (FPIX, ALICE...)

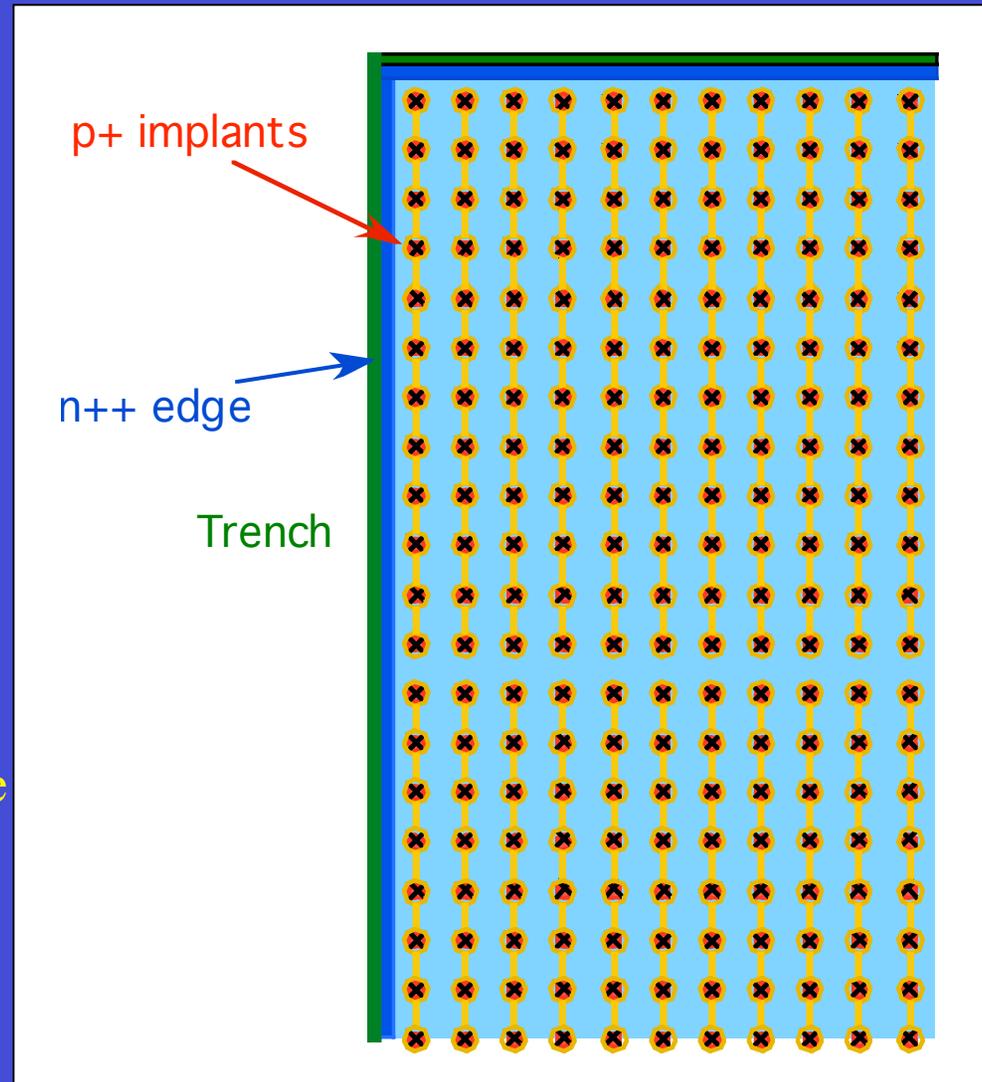
Space Available



Sensor Layout



- 6" wafer, lots of space ...
 - FPIX sensor
 - Alice sensor (p on n)
 - 3D mate
 - Strip detectors
 - Other designs?
- p on n easier for trench processing, simple pixel
- Form strips from pixels
- >30 micron from p+ to sensor edge





SOI Detector + Readout

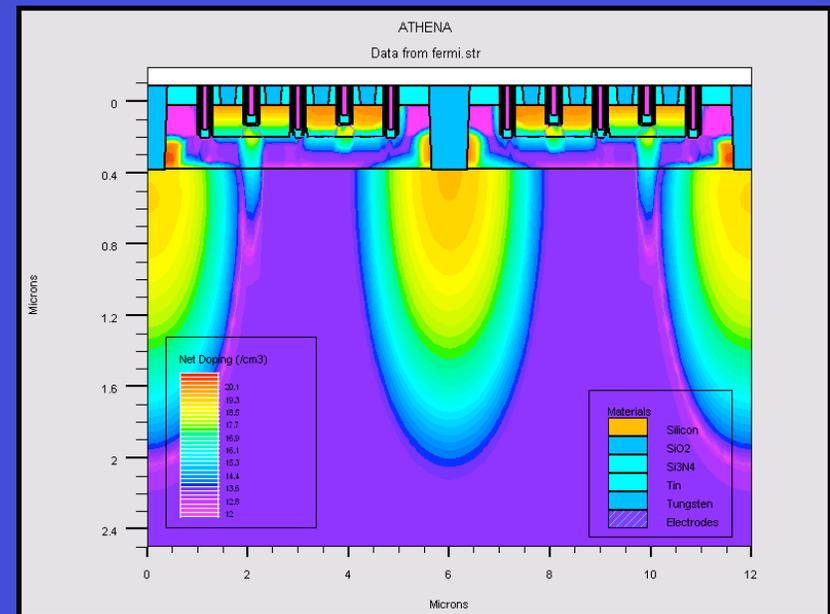
SOI based detectors for HEP have been under study since ~1993

- Pixel is formed on a high resistivity “handle” wafer as part of the device processing
- Basic concepts and techniques similar to 3D (integrate first 2 tiers)

Working with American Semiconductor under SBIR.

- Ability to specify and model processing steps at Cypress
- “FLEXFET” dual gated SOI transistors
- 8” wafers, 0.18 μm SOI CMOS
- ~20 μm pitch pixels, thinned to <100 μm
- Goals

- Model process steps
- Understand+model diode design (pinning, breakdown, via diameter)
- Understand+model handle wafer (resistivity, float zone or CZ ...)
- Understand thinning and backside implantation (laser anneal, MBE ...)
- Design and simulate readout circuit, radiation effects



FLEXFET diode simulation



Non-SOI 3D Processes

Similar techniques can be applied to non-SOI circuits.

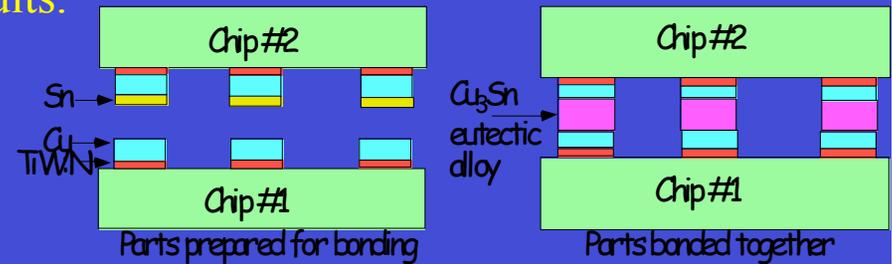
Face to back devices must fabricate insulated vias through the silicon substrate.

Initial studies:

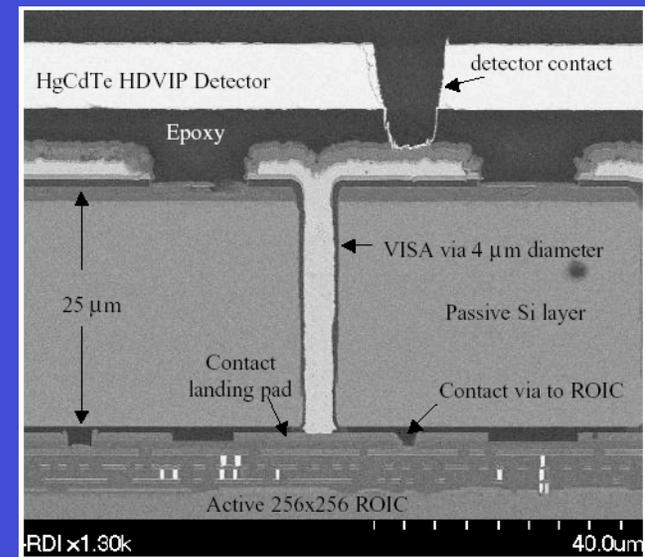
- Thin BTEV pixel FPIX ROIC (50 x 400 um pixels) as small as possible (down to ~15 um) and study performance. (at RTI)

Follow-on work:

- Add Cu/Sn to ROIC pads and Cu to detector pads.
- Perform die to wafer bonding.
- Evaluate eutectic bonding techniques



Face to face example



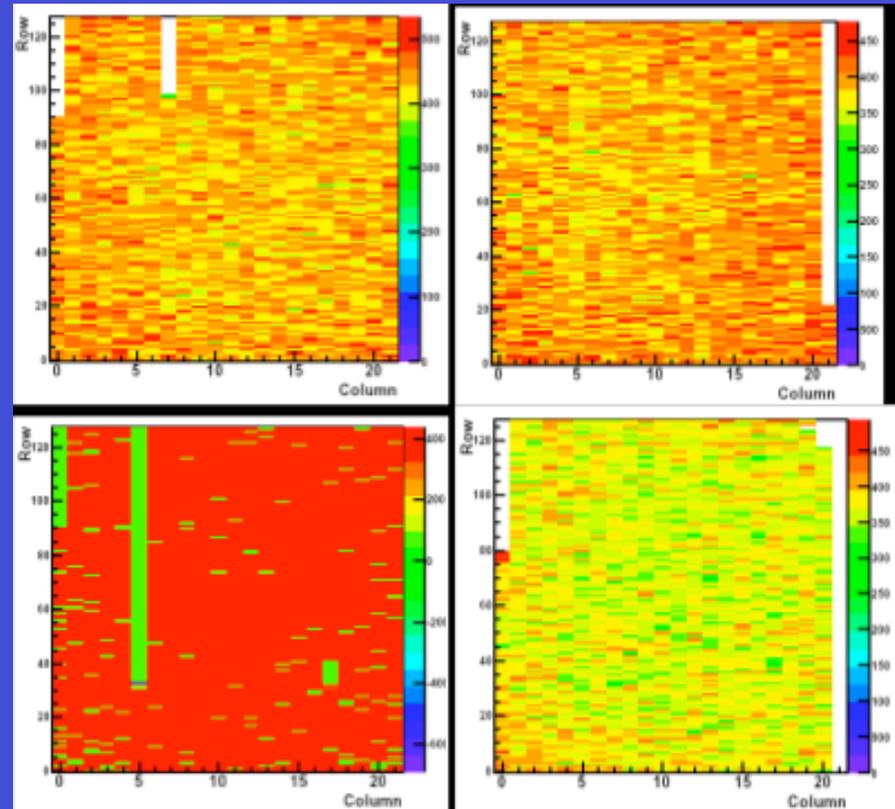
Face to back example (RTI/DRC)

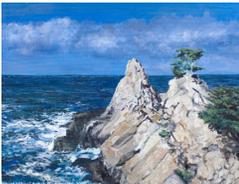
This may be more rad hard than SOI 3D devices (LHC)



Thinning Studies

- As a first pass we have thinned individual BTeV FPIX die to various thicknesses (RTI)
 - Grind to 150 microns
 - Test
 - Plasma etch to final thickness (15-50 microns)
- Initial batch had several problems
 - Low yield (4/20)
 - Cracks
 - Clusters of bad pixels
 - Increased noise
- May be due to improper support during thinning



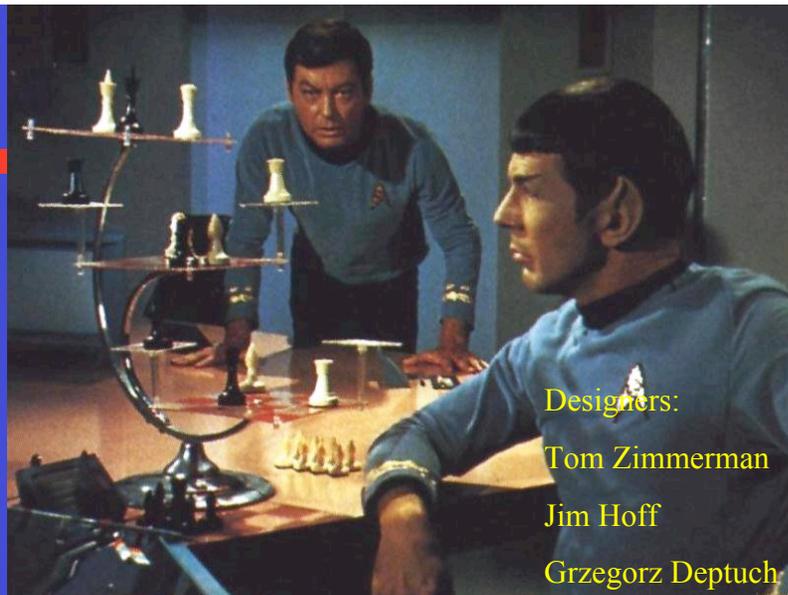


Conclusions

We have *begun* to study new pixel technologies aimed at ILC. Our goal is to demonstrate the viability of 3D technologies for HEP.

1. Three tier 3D readout circuit for MIT-LL multiproject run (10/1)
2. Thinned, edgeless sensors (also with MIT-LL)
 - Mate 3D chips with thinned, edgeless sensors
3. SOI studies with American Semiconductor (SBIR)
4. Effects of thinning on FPIX chip, Cu-Sn 3D technology
 - Mate thinned MIT-LL sensors with FPIX using Cu-Sn bumps ?
 - Mate SOI sensor/RO wafers with custom CMOS tier ?
5. Study system effects (power, interconnections ...)

A combination of these technologies, perhaps with other devices being studied (CCDs, DEPFETs, MAPS) could meet the goals of thin, high resolution detectors, with accurate time stamping and low power.



Designers:
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