Development of 3D Integrated Circuits for HEP

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Outline

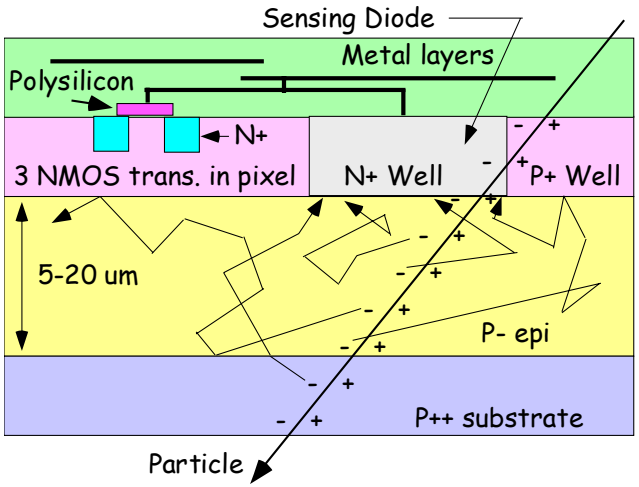
- Brief overview of IC development from MAPS to SOI Detectors to 3D ICs.
- Present several examples of 3D imaging arrays.
- Discuss technologies used for 3D
- Present ILC vertex detector requirements.
- Present a 3D readout chip based on ILC vertex needs.

Introduction

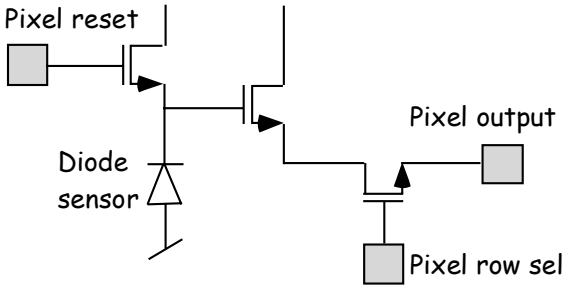
- Requirements for HEP front end electronics and detectors continue to push the limits for lower mass and power, and higher resolution.
- One example is pixel vertex detectors
- Multiple scattering in the detector and the readout electronics limits the precision of particle track reconstruction
  - Therefore very low mass is required.
  - Because low mass is necessary, there is little room for cooling material and hence low power is needed.
  - High resolution requires smaller pixels which increases the readout circuit density.
- Significant progress has been made in the last decade to address these issues by integrating sensors and front end electronics within the pixel cell
  - Monolithic Active Pixel Sensors
  - SOI Pixel Sensors
  - Recent developments in 3D circuits
    - Offers improved performance over other approaches for HEP and other related applications.

MAPS Development

- Monolithic Active Pixel Sensors have generated a lot of interest and excitement in High Energy Physics [1, 2]
  - Combine detector and front end electronics on same substrate in a commercial CMOS process (low resistance substrate).
  - Some issues
    - Relatively small signal level
    - Pixel electronics generally limited to NMOS devices in P-well
    - Limited functionality possible in small pixels
- Currently numerous groups are working on MAPS



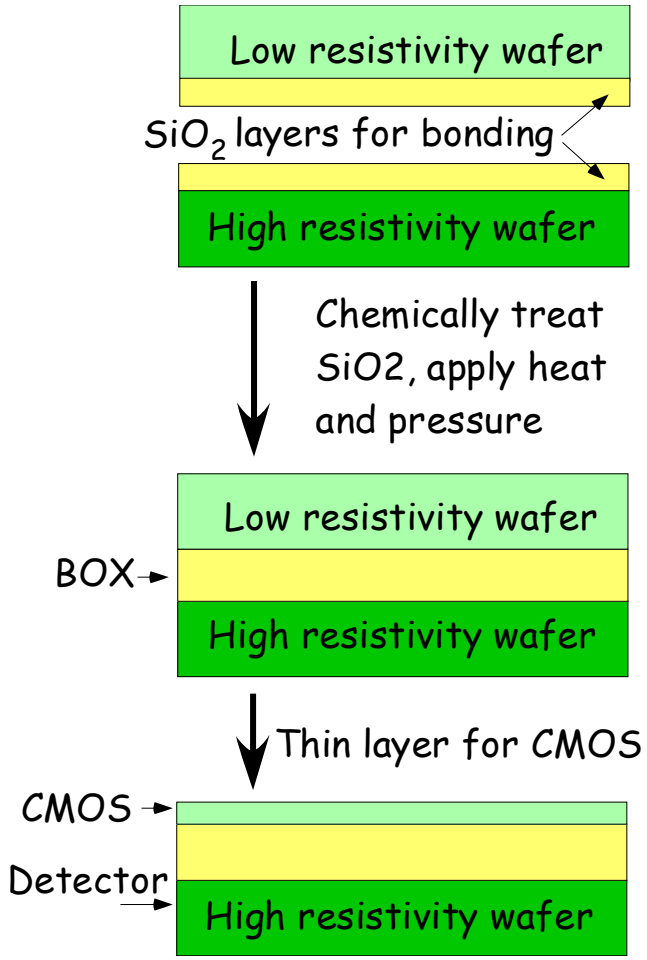
Pixel Cross Section (not to scale)



3 NMOS transistors in Pixel

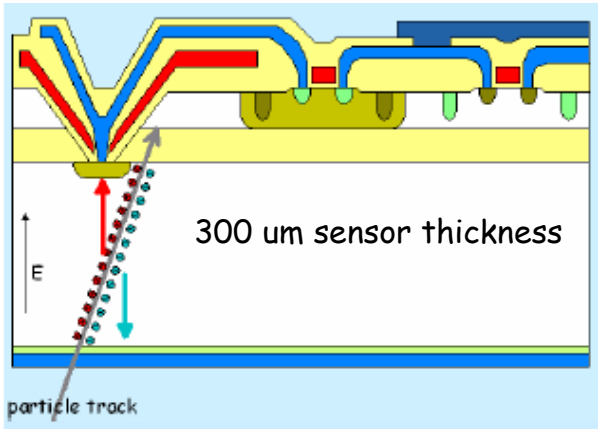
SOI Detector Development

- Wafers for SOI detectors are formed by bonding wafers with low and high resistivity using a silicon oxide bond.
- A buried oxide layer is formed between the wafers
- After bonding, the wafer intended for CMOS processing is thinned to a few microns and small vias are etched through the low resistivity layer and BOX to the high resistivity layer.

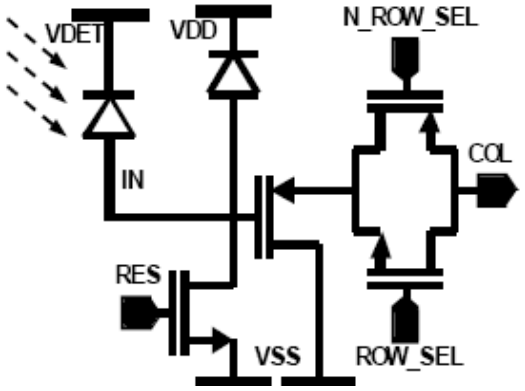


SOI Active Pixel Sensors

- SOI APS have advantages over MAPS
  - CMOS instead of NMOS in pixel
  - Larger signal proportional to high resistivity substrate thickness.
  - Less charge spreading
- Early work done in 3 μm process[3]
  - Large pixels cells not useful for high resolution detectors
- Recent work has moved to smaller feature processes => smaller pixels
  - Collaboration of many groups using the OKI 0.15 μm SOI[4]
  - Fermilab has an arrangement to work with the ASI (American Semiconductor Inc.) 0.18 μm process and OKI on SOI detector development
- SOI offers improved pixel design but still has rather limited functionality within pixel cell.



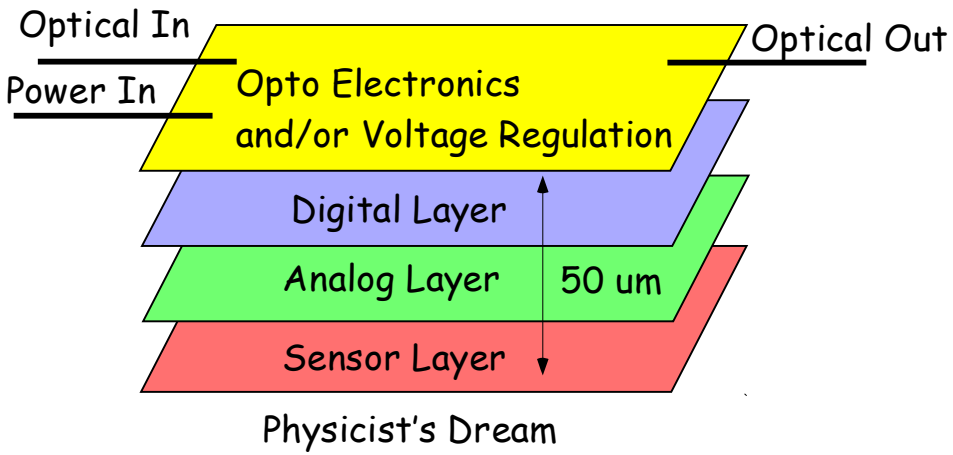
SOI Pixel Cross Section[7]



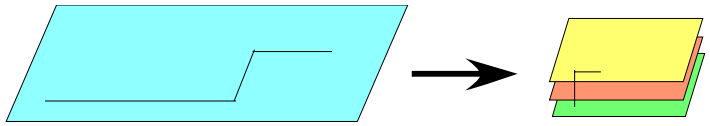
CMOS Transistors in Pixel[7]

3D Integrated Circuit Development

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a "monolithic" circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk



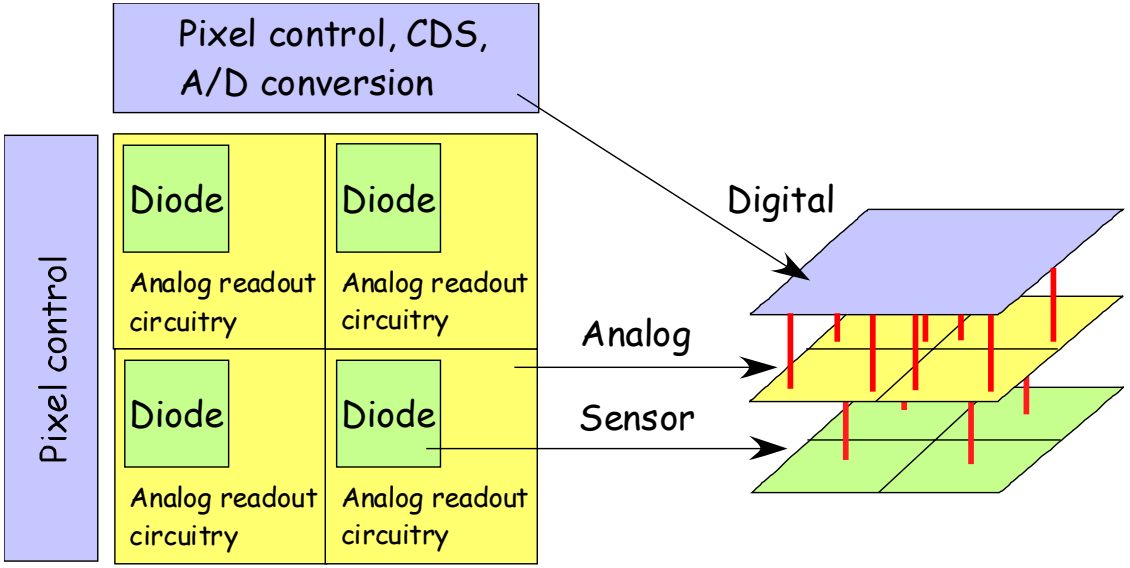
Physicist's Dream



2D Routing (large chip) 3D Routing (small chip)

Advantages of 3D for Pixels

- Significantly higher functionality in a pixel cell
- NMOS and PMOS transistors
- Minimal perimeter area requirements
- Processing of each layer can be optimized
- 3D process is well suited to electronics for pixel arrays



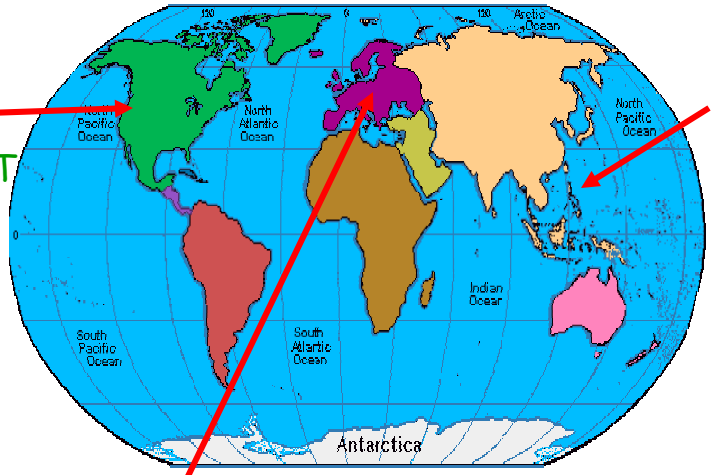
Conventional MAPS 4 Pixel Layout

3D 4 Pixel Layout

3D Integrated Circuit Design

3D electronics development is being pursued by many different organizations.

USA:
Albany Nanocenter, AT&T
BeSang Inc.,IBM, Intel,
Irvine Sensors
Jazz Semiconductor,
Lincoln Labs, MIT,
Micron, RPI, RTI,
Sandia Labs
Tessera, TI, Tezzaron,
U. Of Kansas,
U of Arkansas
Vertical Circuits, Ziptronix



Asia:
ASET, NEC, University of Tokyo,
Tohoku University, CREST,
Fujitsu, ZyCube, Sanyo,
Toshiba, Denso, Mitsubishi, Sharp,
Hitachi, Matsushita, Samsung

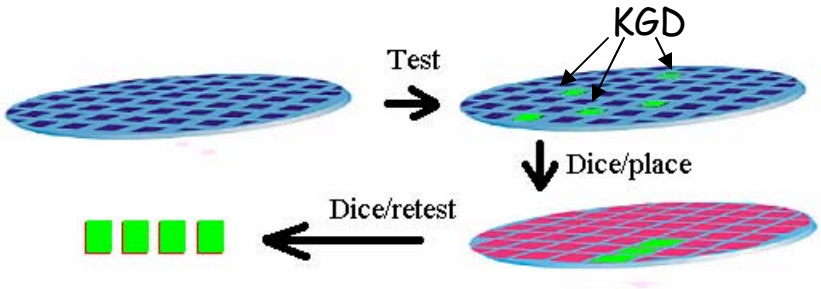
Europe: Alcatel Espace, CEA-LETI, EV Group
EPFL, Fraunhofer IZM, IMEC Delft,
Infineon, NMRC, Phillips, NMRC, STMicroelectronics,
Thales, TU Berlin

Key Technologies for 3D[5]

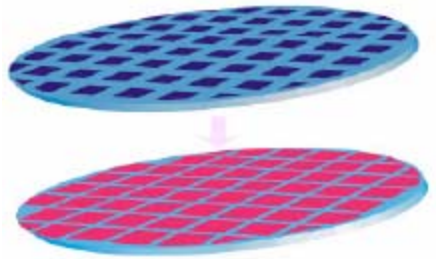
- Bonding between layers
  - Oxide to oxide fusion
  - Copper/tin bonding
  - Polymer bonding
- Wafer thinning
  - Grinding, lapping, etching, CMP
- Through wafer via formation and metalization
  - With isolation
  - Without isolation
- High precision alignment

Two Different 3D Approaches for HEP

1) Die to wafer, (or die to die) bonding
   - Permits easy usage of different processes and different size wafers (SOI+CMOS, CCD+CMOS, DEPFET+CMOS)
   - Lends itself to using KGD for higher yields
2) Wafer to wafer bonding using SOI
   - Permits very thin layers for reduced mass
     - Short, small vias
   - Layers must align at the wafer level



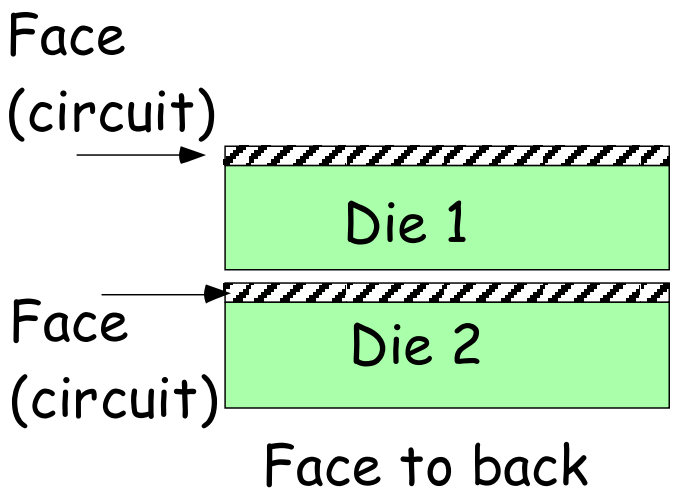
Die to wafer bonding



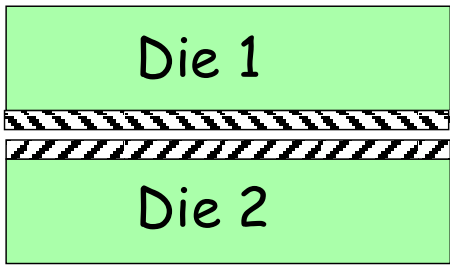
Wafer to wafer bonding

1) Die to Wafer Approach

- Two different types of bonding arrangements are possible.
  - 1) Face to back (circuit side to substrate side)
    - Inter chip vias required for electrical interconnection
  - 2) Face to face
    - Inter chip vias not required
- Examine a couple of bonding arrangements for die to wafer approach.



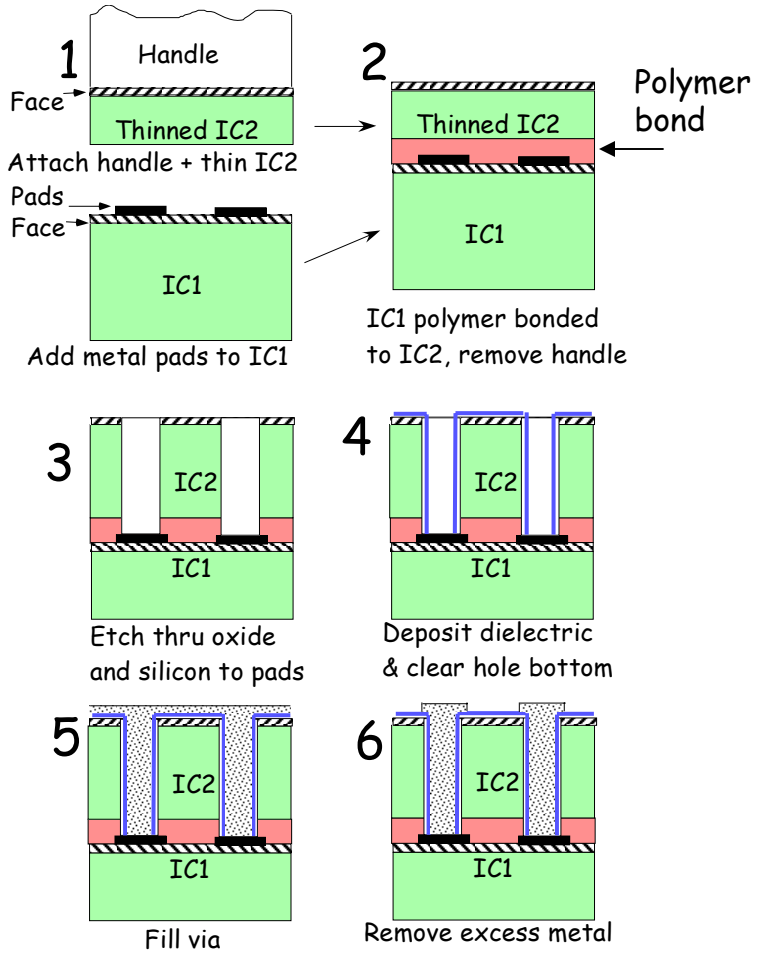
Face to back



Face to face

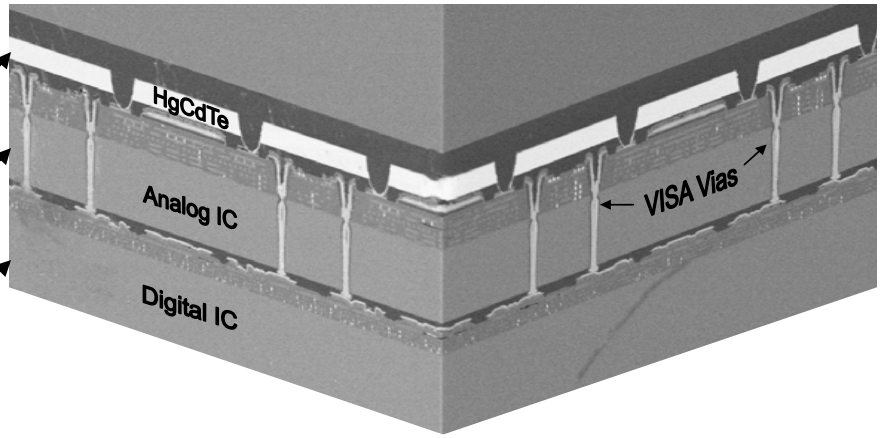
Die to Wafer (back to face)

- Need to leave space in design for vias
- Thin die before bonding (1)
- Polymer bond between parts (2)
- High aspect ratio via Bosch process (3)
- Insulated vias needed for CMOS (4)
- Low temperature via metalization needed to protect polymer bond (5,6)
- Variations of this process are found in different groups (copper vias)

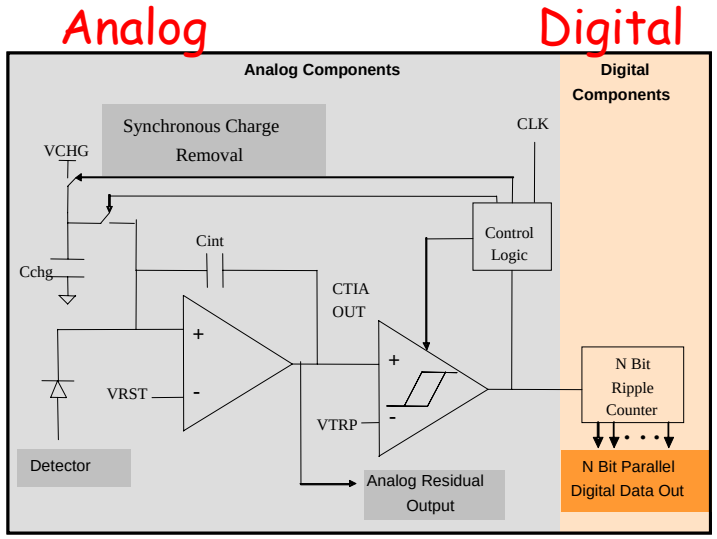


RTI 3D Infrared Array Example[6]

- 256 x 256 array with 30 μm pixels
- 3 Tiers
  - HgCdTe (sensor)
  - 0.25 μm CMOS (analog)
  - 0.18 μm CMOS (digital)
- Die to wafer stacking
- Polymer adhesive bonding
- Bosch process vias (4 μm) with insulated side walls
- 99.98% good pixels
- High diode fill factor



Array cross section

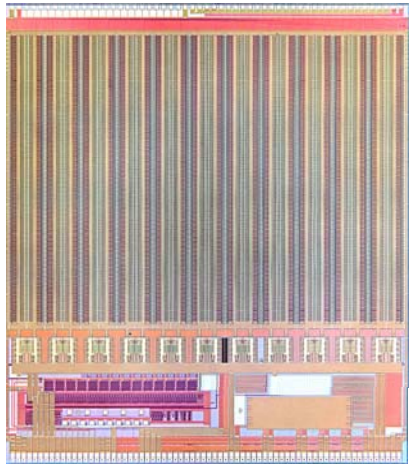


3 Tier circuit diagram

Infrared image

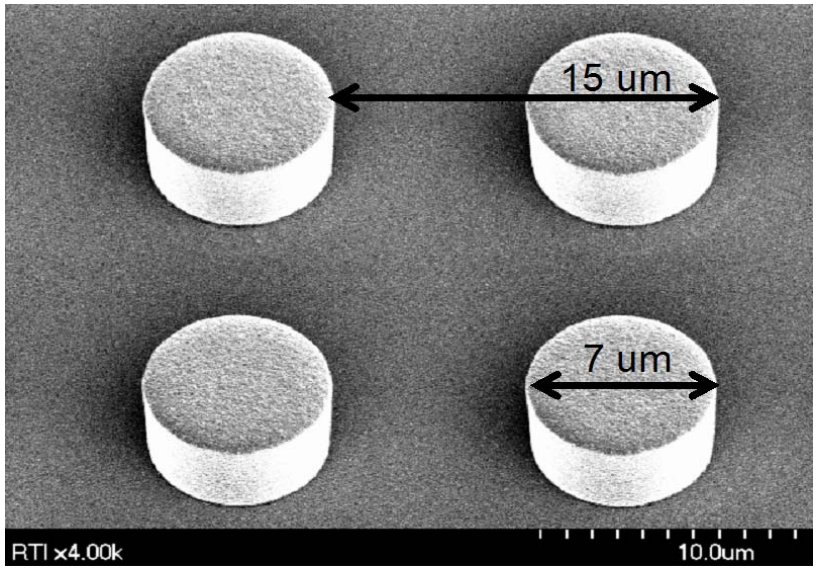
Die to wafer (face to face)

- Use copper-tin eutectic bond for electrical and mechanical connection
- Possible replacement for bump bonds
- In applications to date, the copper interconnect is 10 um thick and covers most of surface area.
  - Problem for HEP: 10 um Cu => Xo = 0.07%
- Fermilab study
  - Thin FPIX parts (TSMC 0.25 um process) down to 15 microns. Reasonable success for first attempt.
  - Bond FPIX parts to detectors using Cu+Sn.
  - Reduce copper coverage to 10% of surface area to minimize Xo for mass critical applications
  - Attempt 7 um diameter interconnect on 20 um pitch.

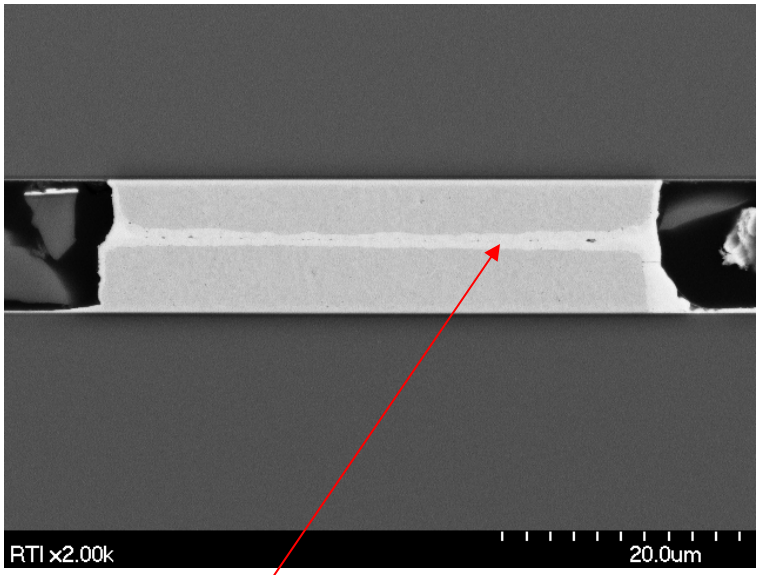


FPIX

Fine Pitch CuSn Pillars from RTI for Bonding Along with Cross Section to Show Eutectic Bond



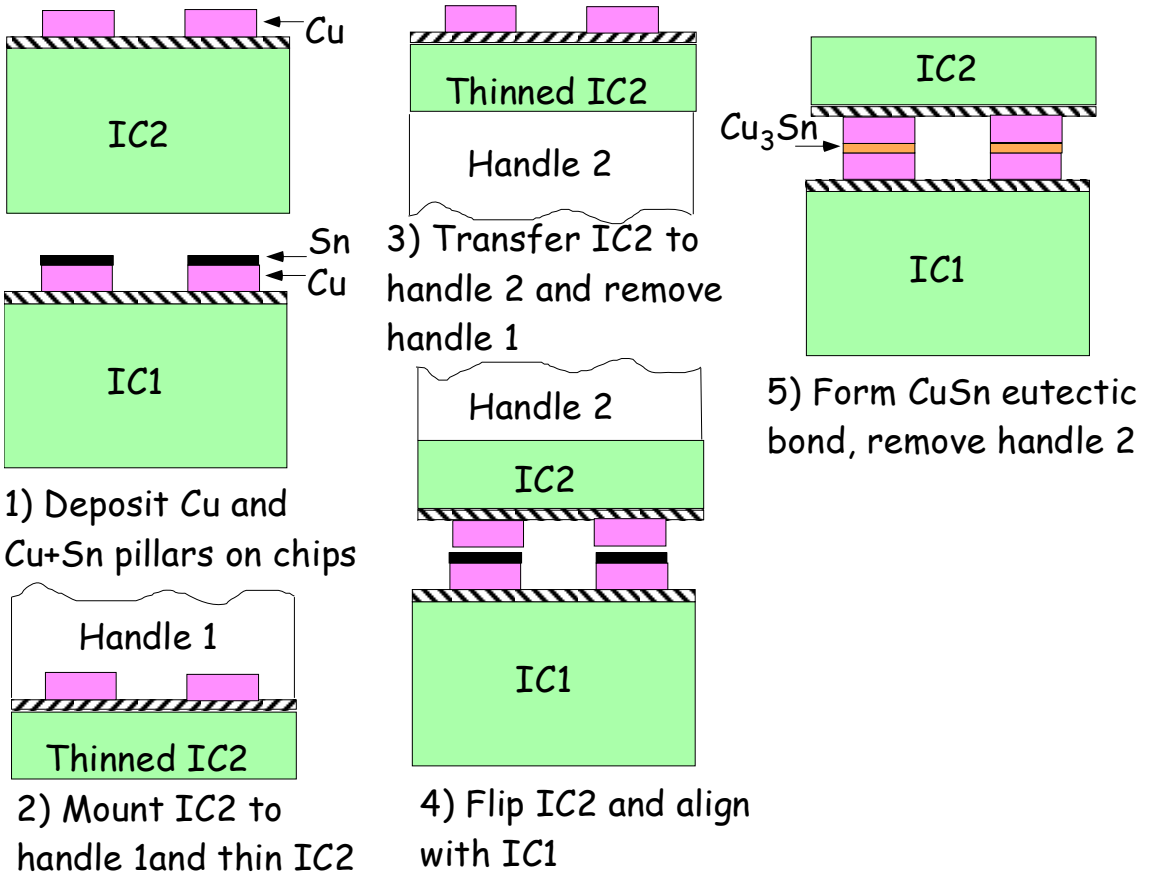
5 micron tall Cu pillars



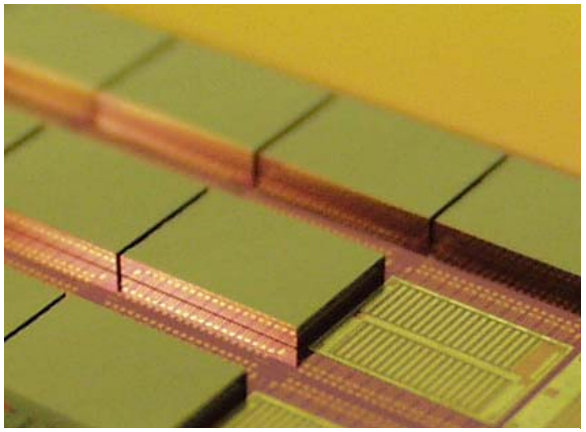
Cross section of bond showing Cu_3Sn eutectic

Cu/Sn Bond process

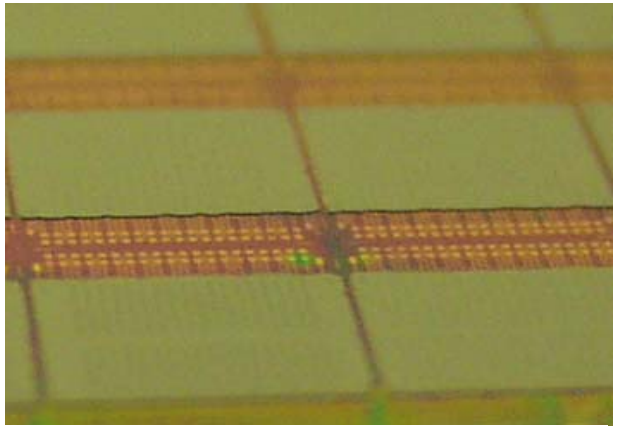
- Cu pillar placed on face of one device and copper pillar with Sn on other (1).
- Requires double handle wafer transfer (2, 3).
- Cu and Sn form eutectic bond between devices (4, 5)
- Variations of this process are found in different groups
- Process is compatible with standard CMOS processing



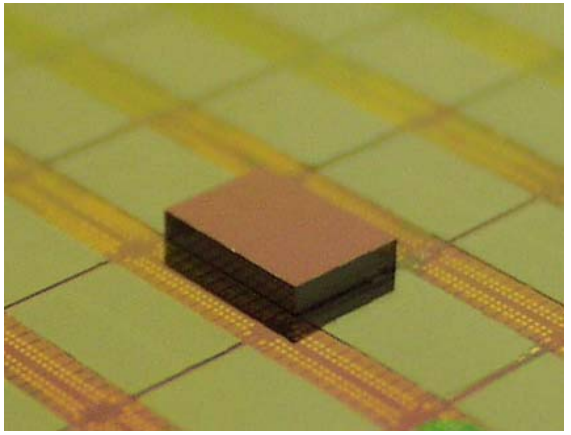
Thinned Die Photos from IZM[7]



500 μm thick chips placed on target Substrate using CuSn eutectic bond



Chips thinned to 10 μm on target substrate



500 μm chip placed on top of 10 μm thick chips for comparison.

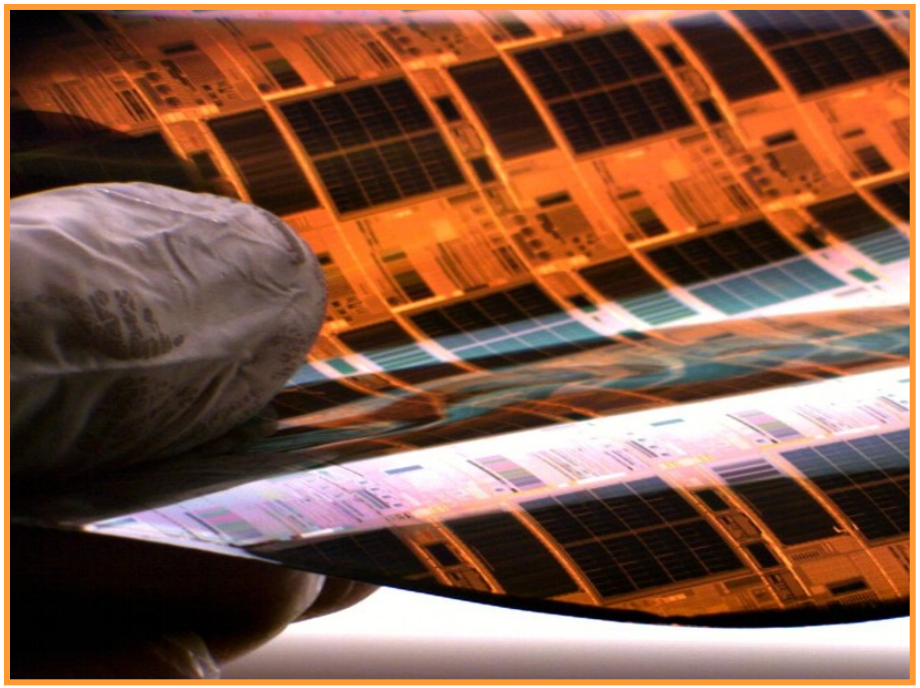
2) Wafer to Wafer Bonding

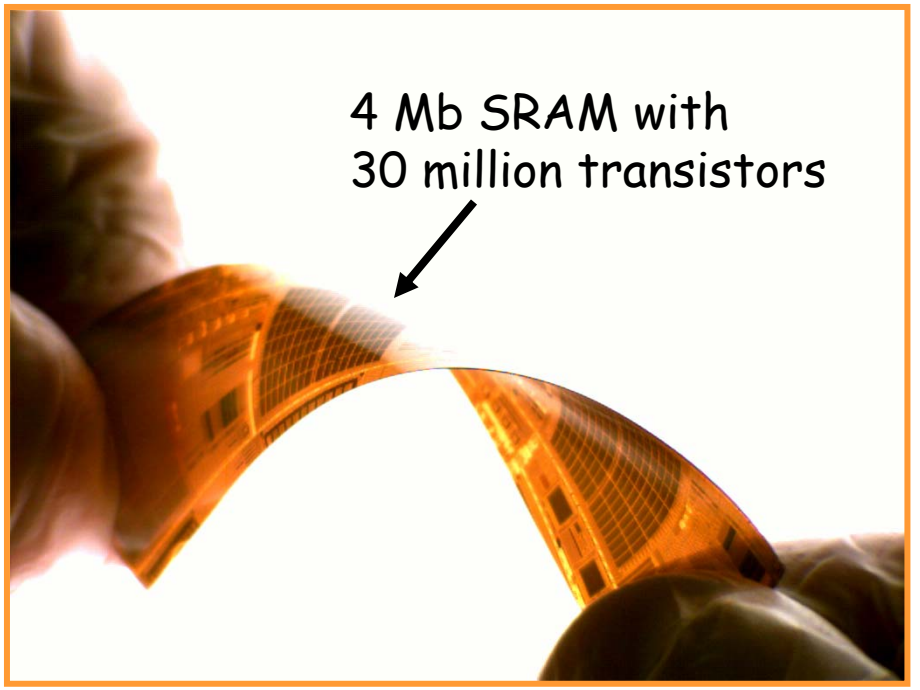
- Wafers are joined together using SiO_2 bond.
- Similar technique is used to bond wafers for SOI detector development previously mentioned.
  - For SOI detector design, processing of both wafers is done after bonding
  - For 3D circuit design, processing of each wafer is done before bonding.
- Examine bonding of SOI wafers in MIT Lincoln Labs 3D process.

3D SOI Wafer Processing

- Each wafer is easily thinned to the buried oxide layer (BOX) since the buried oxide acts as an etch stop.
- Wafers have been thinned to 6 microns.
- Inter wafer vias do not need to be insulated since they pass through insulating oxide.
- Thin wafers permit short vias which result in smaller diameter vias and more room for circuitry.

Thinned SOI Wafers

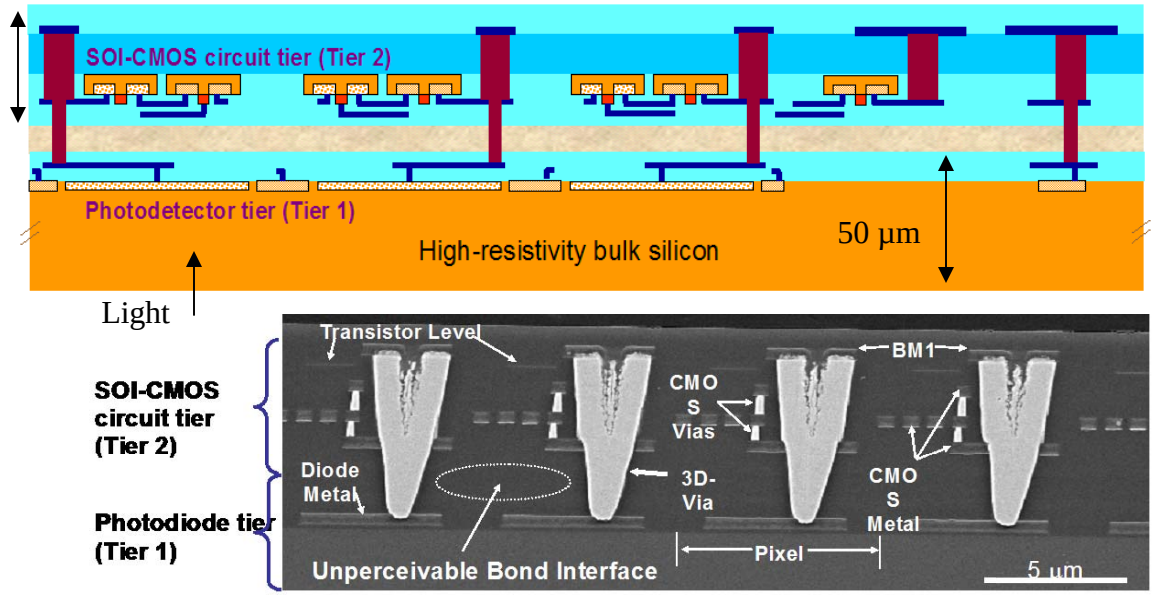




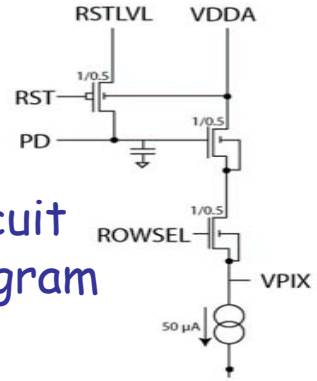
Wafer thinned to 6 microns and mounted to 3 mil kapton (MIT LL)

3D Megapixel CMOS Image Sensor[8]

- 1024 x 1024, 8 μm pixels
- 2 tiers
- Wafer to wafer stacking (150 mm to 150 mm)
- 100% diode fill factor
- Tier 1 - p+n diodes in >3000 ohm-cm, n-type sub, 50 μm thick
- Tier 2 – 0.35 um SOI CMOS, 7 μm thick
- 2 μm square vias, dry etch, Ti/TiN liner with W plugs
- Oxide-oxide bonding
- 1 million 3D vias
- Pixel operability >99.999%
- 4 side abuttable array



Drawing and SEM Cross section

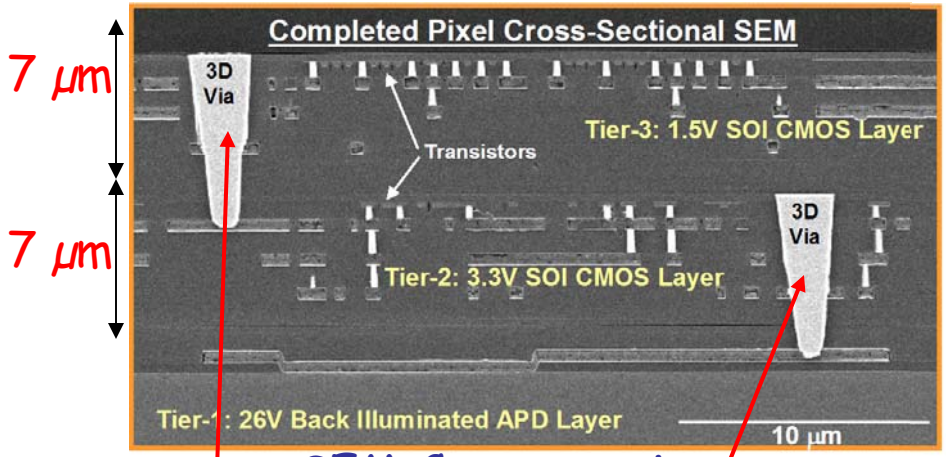


Circuit Diagram

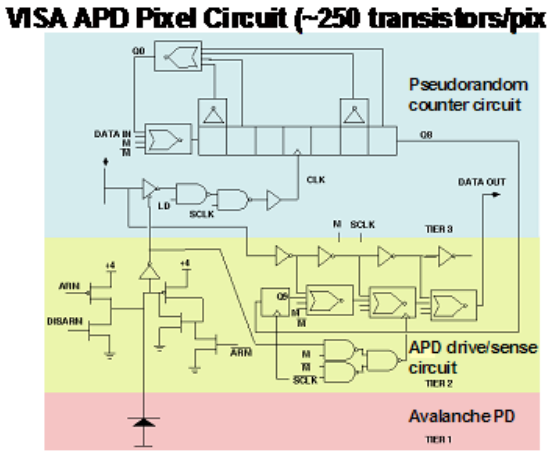
Image

3D Laser Radar Imager[9]

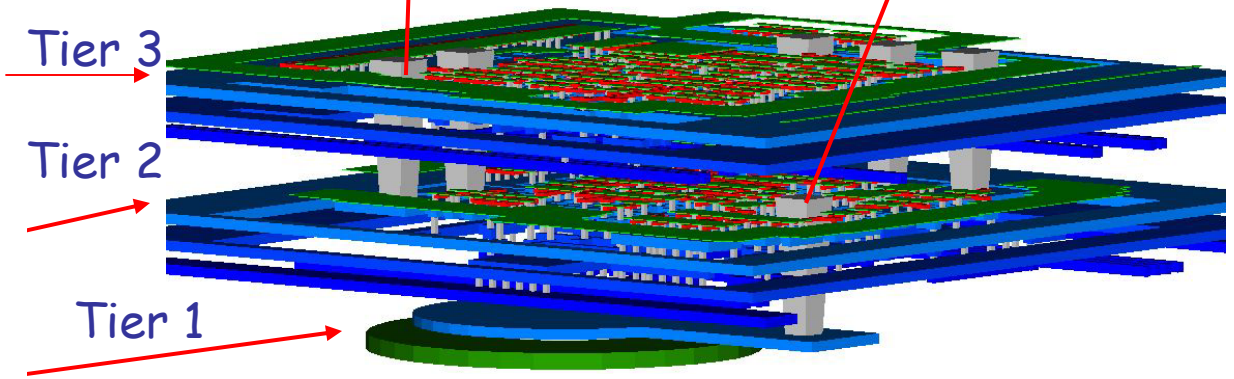
- 64 x 64 array, 50 μm pixels
- 3 tiers
  - 0.18μm SOI
  - 0.35 μm SOI
  - High resistivity substrate diodes
- Oxide to oxide wafer bonding
- 1.5 μm vias, dry etch
- Six 3D vias per pixel



SEM Cross section



Schematic

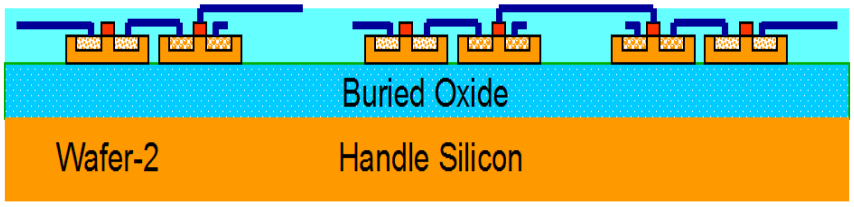


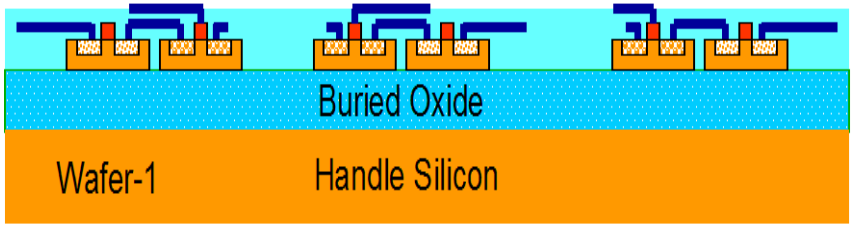
CAD Drawing

3D SOI Process Flow[10]

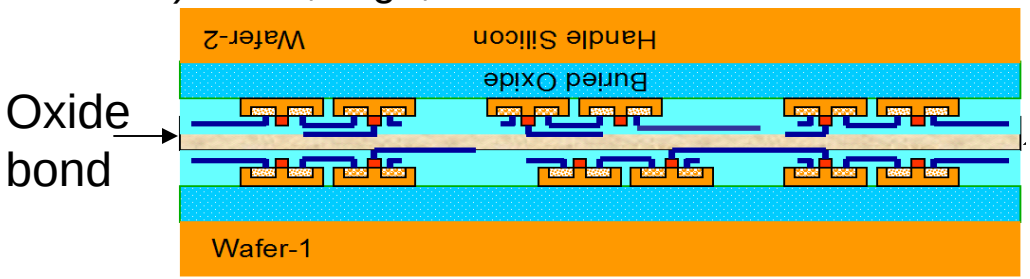
- MIT LL process
- 3 tier stacking
- 6 inch 0.18 um SOI wafers

1) Fabricate individual tiers

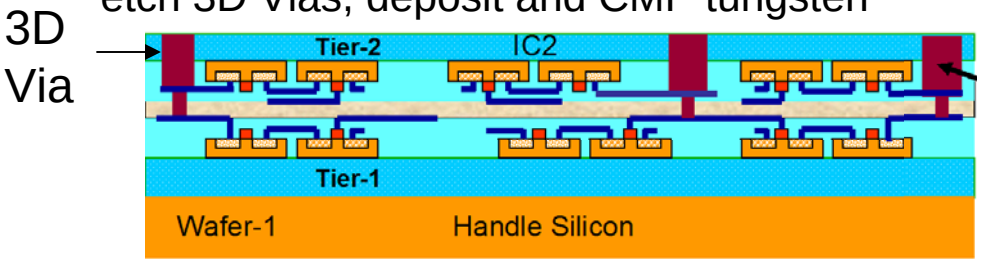




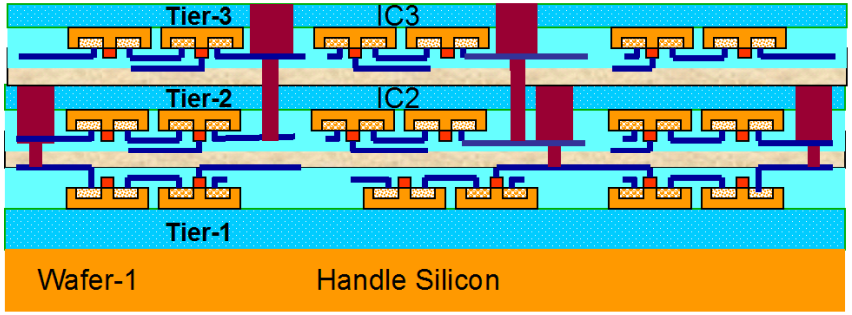
2) Invert, align, and bond wafer 2 to wafer 1



3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



3D Demonstrator Chip for ILC Pixels

- ILC expected to have beam structure with 2820 crossings in a 1 msec bunch train with 5 bunch trains/sec.
- ILC Maximum hit occupancy
  - Assumed to be 0.03 particles/crossing/mm^2
  - Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)
  - Hit rate = 0.03 part./bco/mm^2 x 3 hits/part. x 2820 bco/train = 252 hits/train/mm^2. [11]
- Study analog and binary read out approach
  - Want better than 5 μm resolution
  - Binary readout
    - 15 um pixel gives 15/$\sqrt{12}$ = 4.3 um resolution
    - 20 um pixel gives 5.8 um resolution

Requirements for Sparsification, Time Stamping, and Pipeline Depth

- Sparsification is highly desirable to reduce the volume of data being transmitted off any chip and to reduce the digital power dissipated in the chip.
- Although the ILC pixel occupancy is relatively low, Time Stamping is necessary to define when a hit in occurred in a given pixel in order to reconstruct a hit pattern in association with data from other detectors.

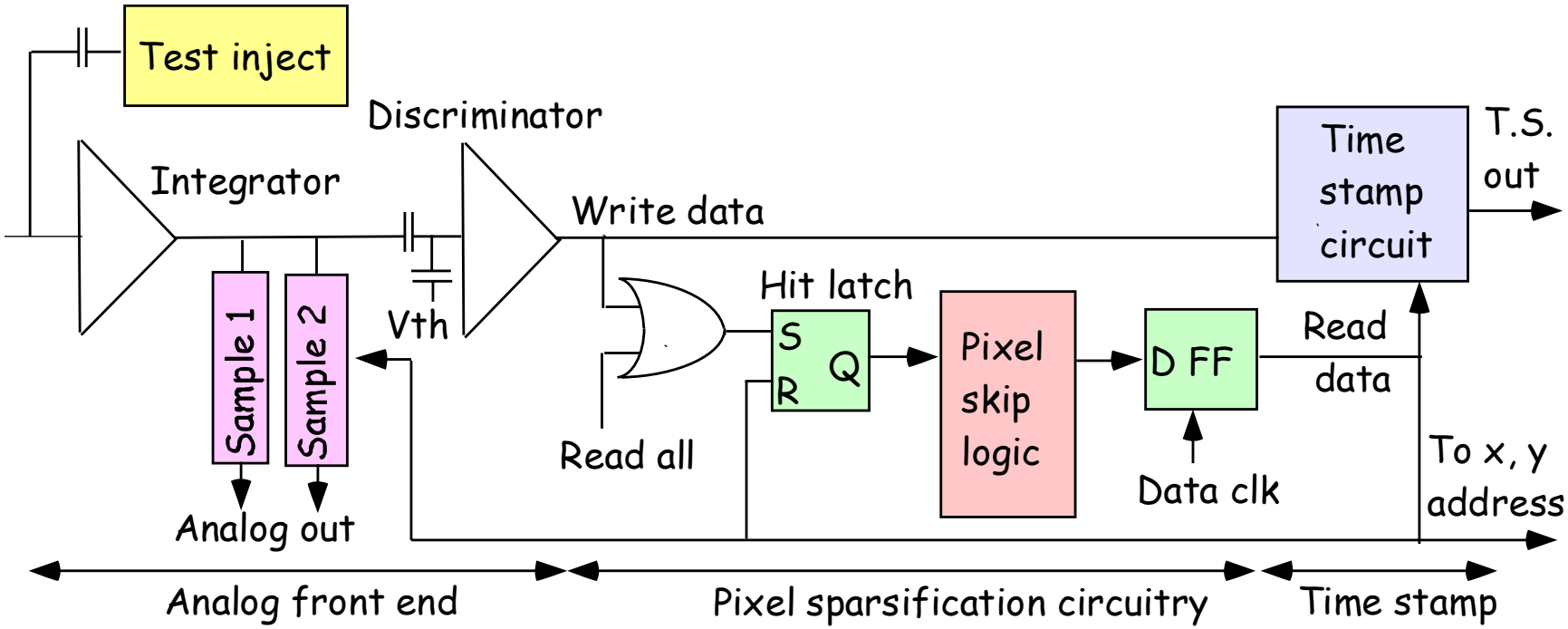
Requirements (continued)

- Occupancy in a pixel for 2820 bco
  - Occupancy in 15 μm pixel = 250 hits/mm^2 x (15μm x 15μm) = 0.056 hits/bunch train
    - Chance of a single cell being hit twice in a bunch train = .056 x .056 = .0031 => 0.3%
    - Therefore, with a pipeline depth of only one, 99.7% of hits are recorded unambiguously.
  - Occupancy in a 20 μm pixel = 0.1
    - Chance of a cell being hit twice in a bunch train = 0.1 x 0.1 = 0.01 =>1.0%
    - Therefore, with a pipeline depth of only one, 99% of hits are recorded unambiguously.

Demonstrator Chip Design Choices

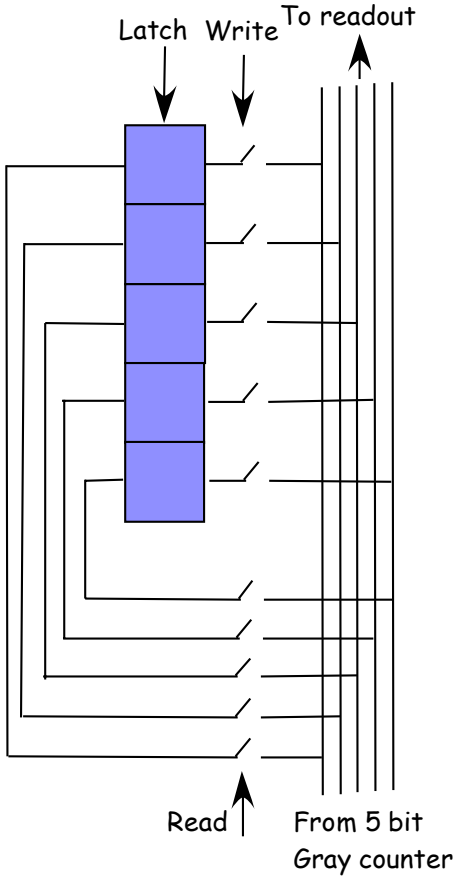
- Provide analog and binary readout information
- Divide the bunch train into 32 time slices. Each pixel stores one time stamp equivalent to 5 bits of time information.
- Store the time stamp in the hit pixel cell.
- Use token passing scheme with look ahead feature to sparsify data output.
- Store pixel address at end of row and column.
- Divide chip design into 3 tiers or layers of ROIC
- Make pixel as small as possible but with significant functionality.
- Design for 1000 x 1000 array but layout only for 64 x 64 array.

Simplified Pixel Cell Block Diagram



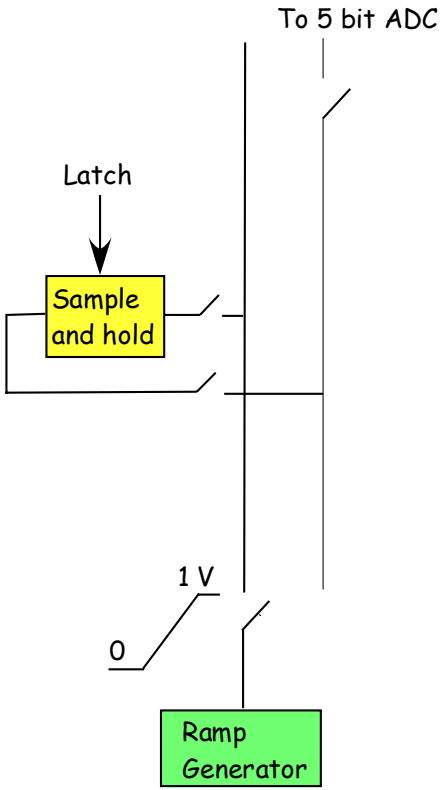
Pixel Time Stamping

- Various MAPS schemes for ILC have suggested 20 time stamps to separate hits in the 2820 bunch train.
- ILC 3D chip has 32 time stamps.
- Time stamp can be either analog or digital.
- ILC demonstrator chip will have both



Counter operates at a slow speed, 32 KHz, (30 usec/step)

All digital - 10 transistors/bit

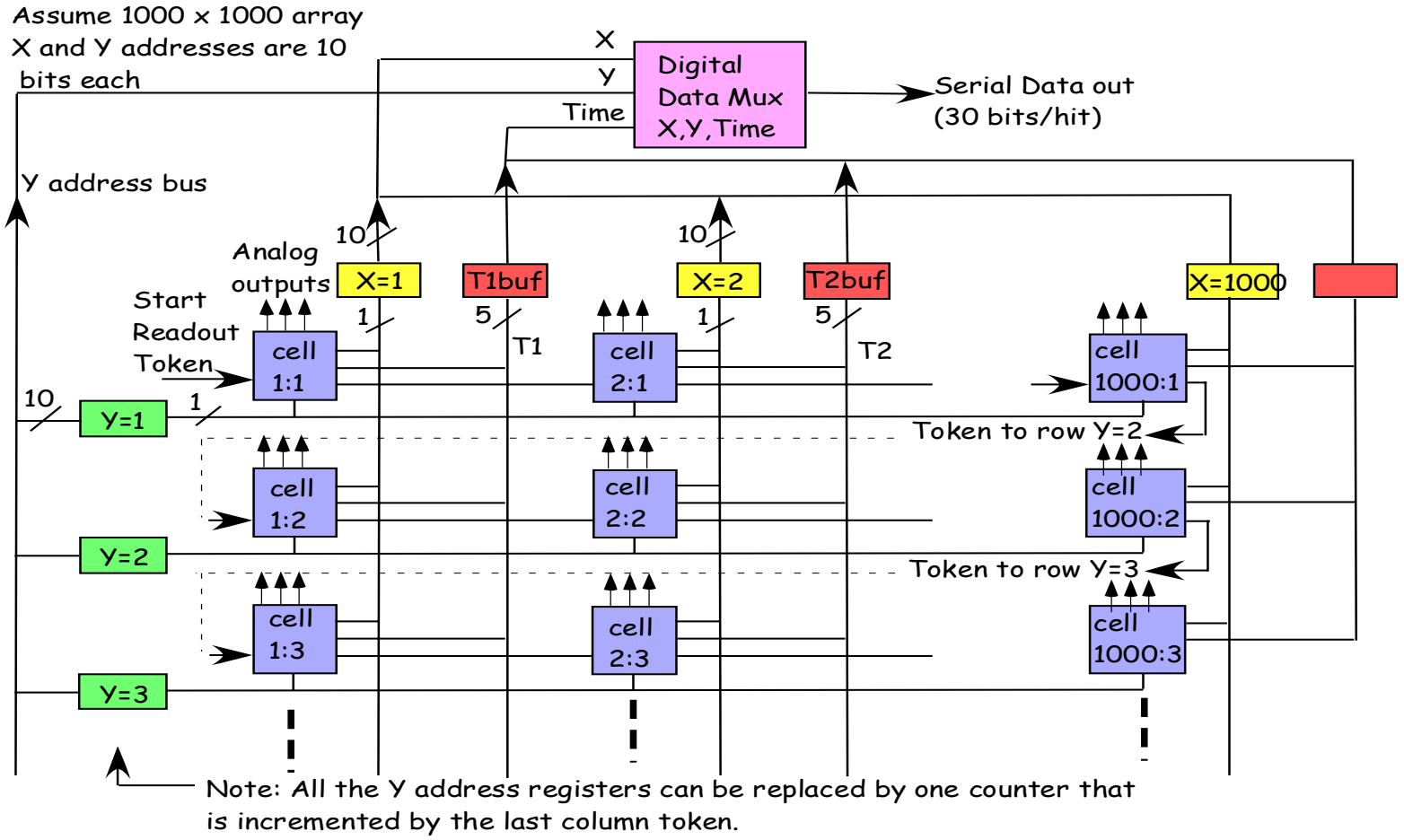


Ramp operates at low speed for low power.

Analog approach - fewer transistors

Pixel Readout Scheme

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out.
- During pixel readout, token scans ahead for the next hit pixel



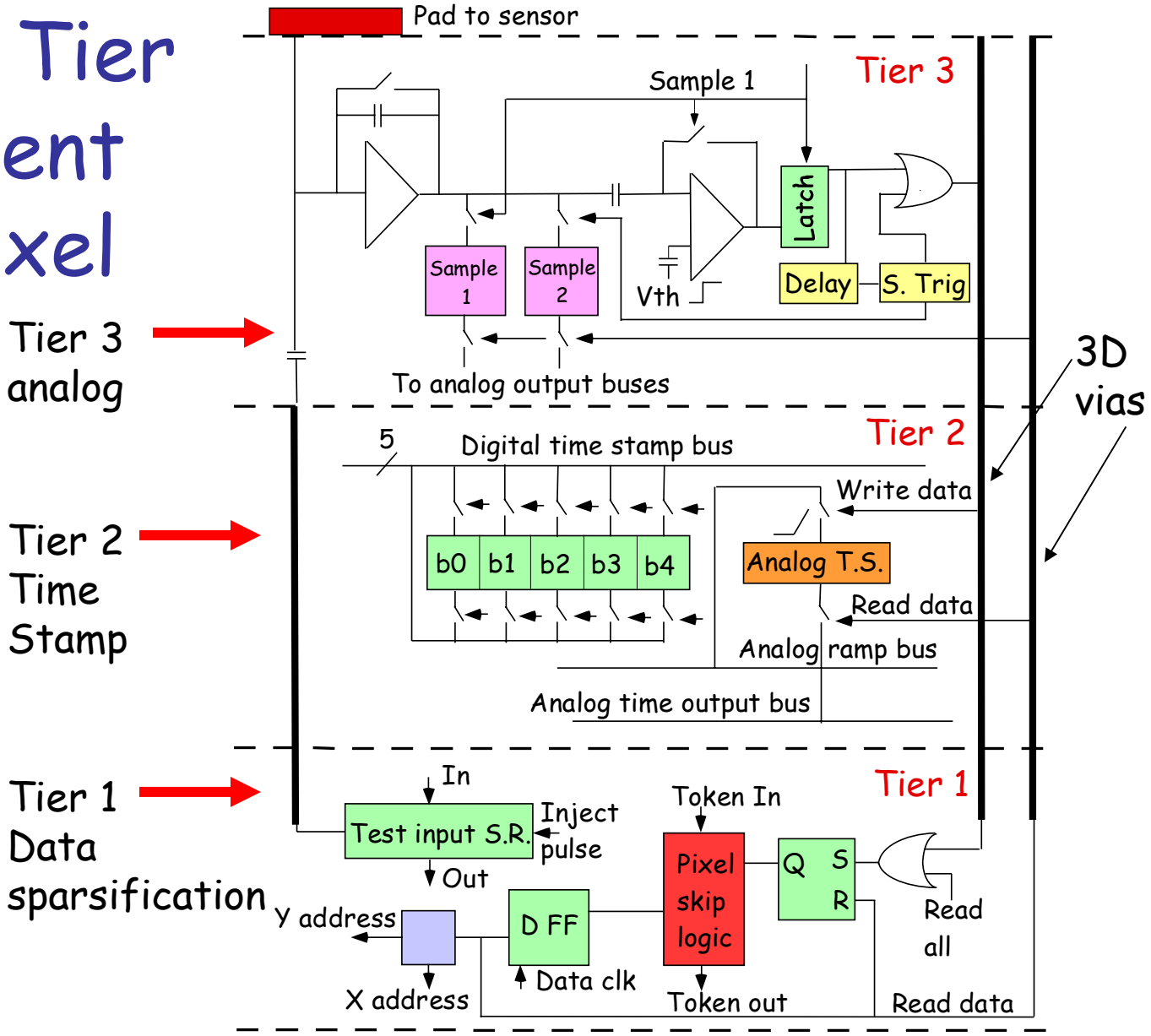
Sparsified Readout Operation

- During data acquisition, a hit sets a latch.
- Sparse readout performed row by row.
- To start readout, all hit pixels are disabled except the first hit pixel in the readout scan.
- The pixel being read points to the X address and Y address stored on the perimeter and at the same time outputs the Time Stamp and analog information from the pixel.
- While reading out a pixel, a token scans ahead looking for next pixel to readout.
- Chip set to always readout at least one pixel per row in the array.
- Assume 1000 x 1000 array (1000 pixels/row)
  - Time to scan 1 row = .200 ns x 1000 = 200 ns (simulated)
  - Time to readout cell = 30 bits x 20 ns/bit = 600 ns
  - Plenty of time to find next hit pixel during readout

Readout Time Example

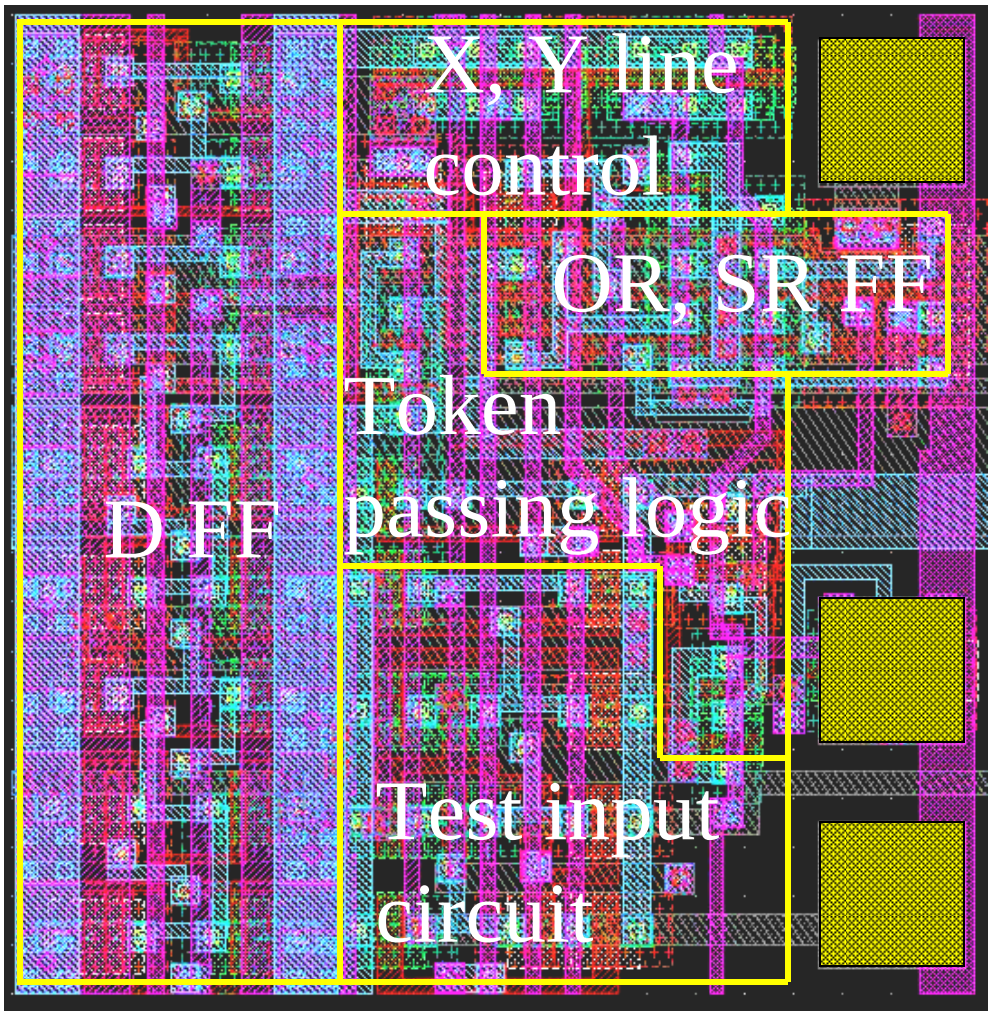
- Chip size = 1000 x 1000 pixels with 15 um pixels.
- Max hits/chip = 250 hits/mm^2 x 225 mm^2 = 56250 hits/chip.
- If you read all pixels with X=1, add 1000 pixels (small increase in readout data).
- For 50 MHz readout clock and 30 bits/hit, readout time = 57250 hits x 30 bits/hit x 20 ns/bit = 34 msec.
- For a 1000 x 1000 array of 20 um pixels, the readout time is 60 usec.
- Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips.
- Digital outputs are CMOS. The output power is only dependent on the number of bits and not the length of time needed to readout.

3D Three Tier Arrangement for ILC Pixel



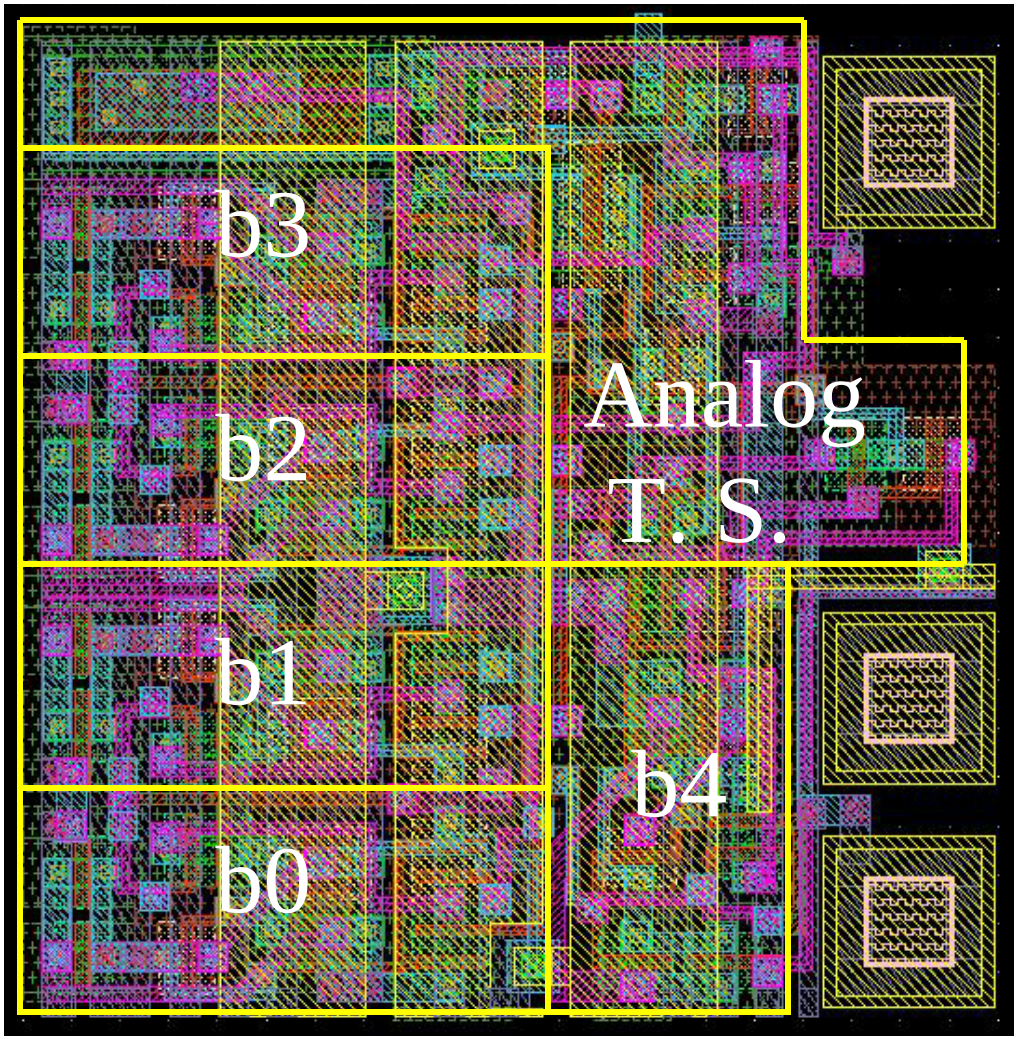
Sparsification Tier 1

- OR for READ ALL cells
- Hit latch (SR FF)
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



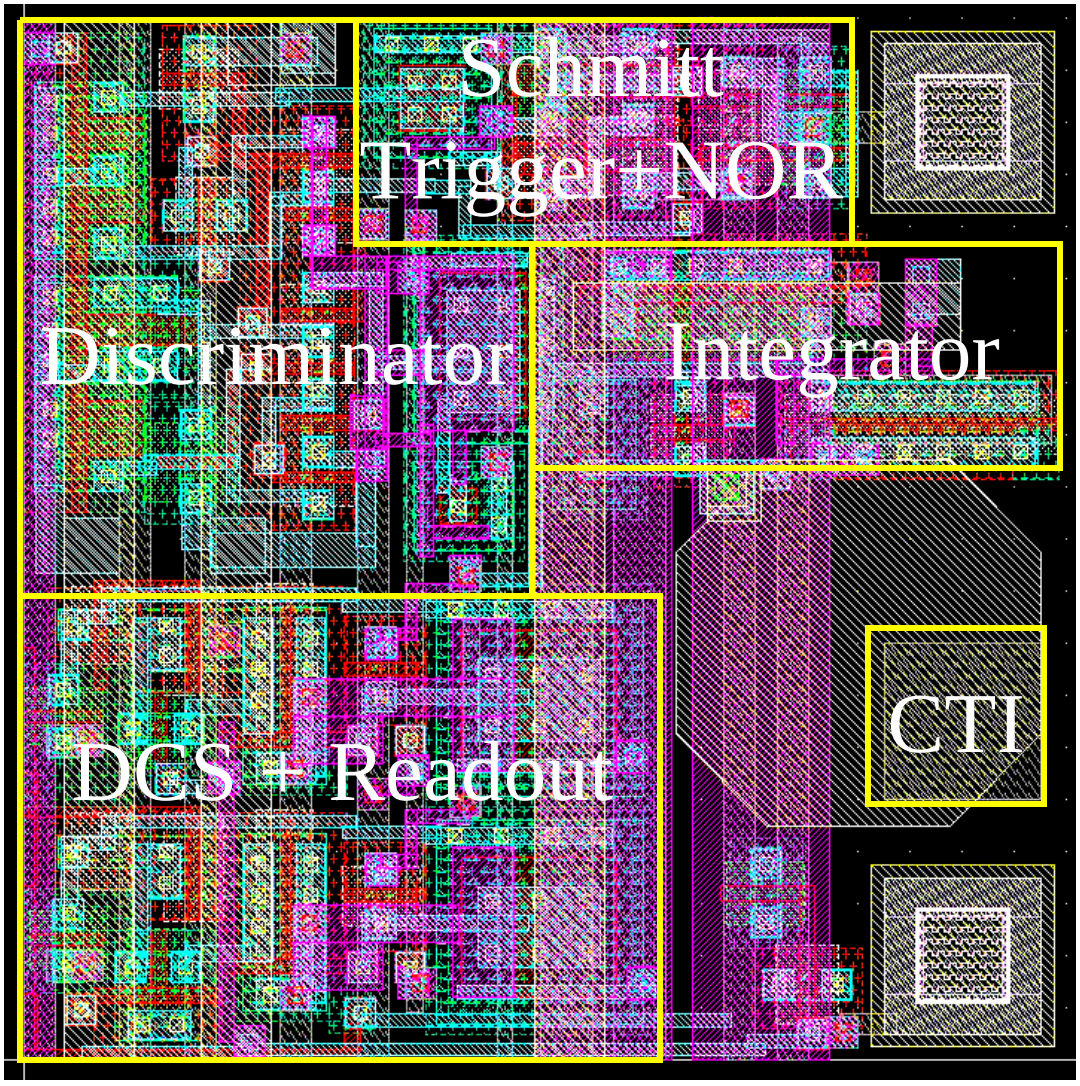
Time Stamp – Tier 2

- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Either analog or digital T. S.to be used in final design.
- Gray code counter on periphery
- 72 transistors
- 3 vias

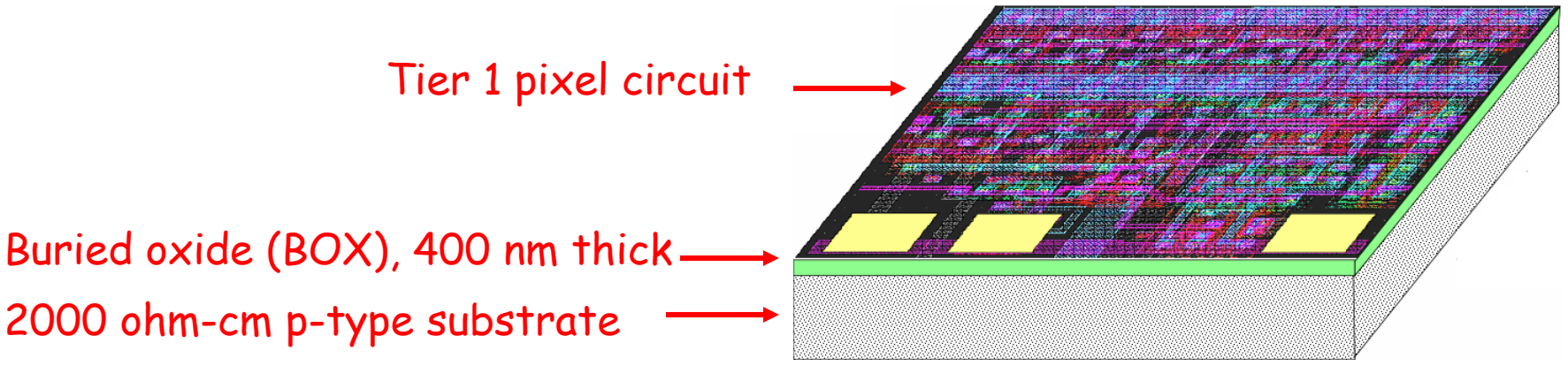


Analog Tier 3

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input (CTI)
- 38 transistors
- 2 vias

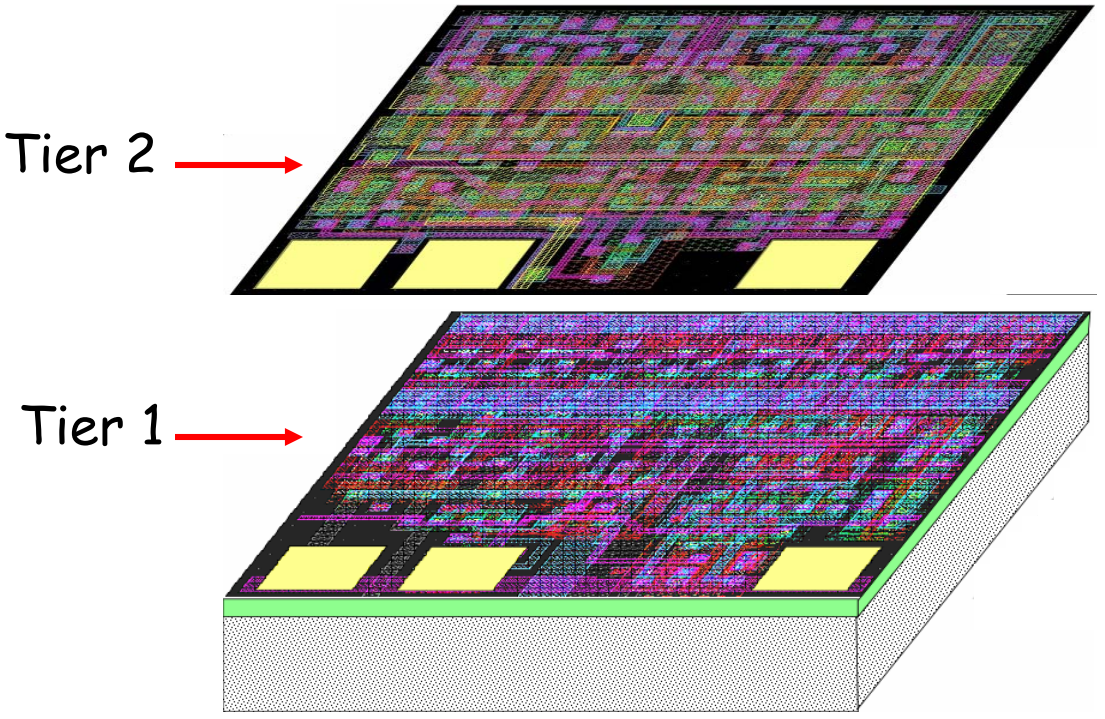


3D Stacking with Vias (step 1)



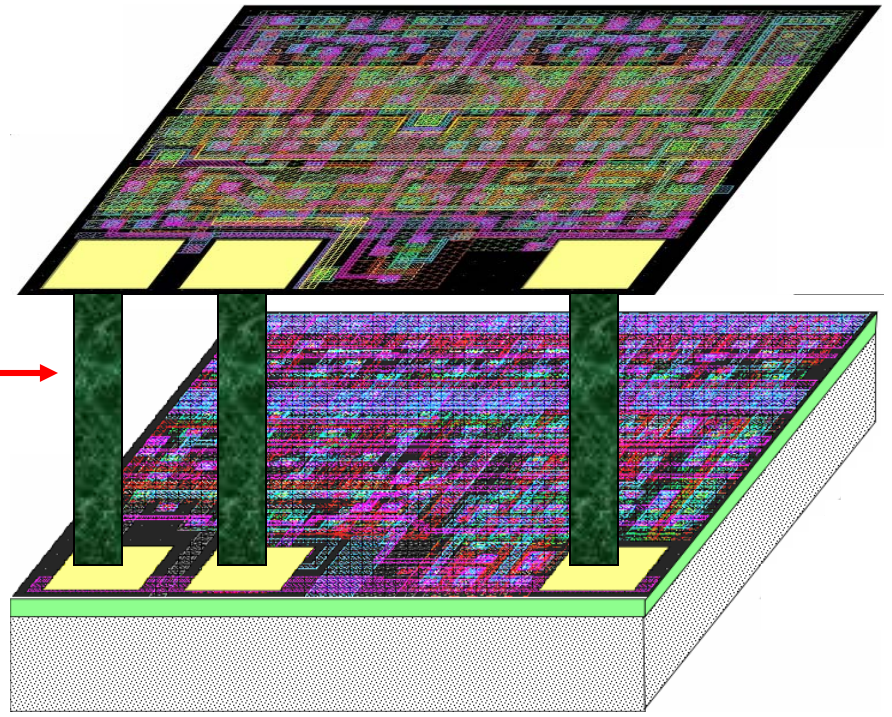
3D Stacking with Vias (step 2)

Bond tier 2 to tier 1



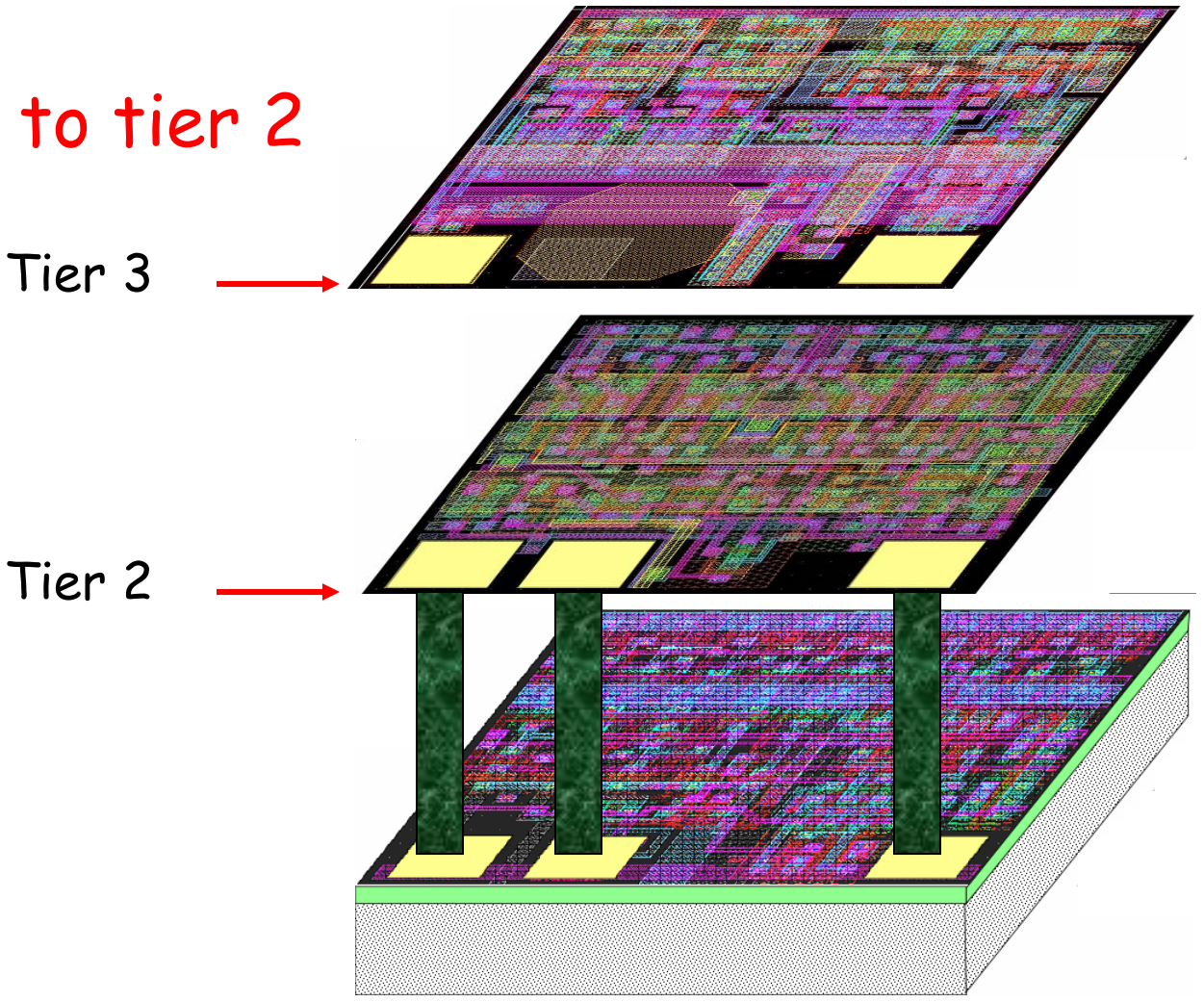
3D Stacking with Vias (step 3)

Form 3 vias, 1.5 x 7.3 μm, through Tier 2 to Tier 1



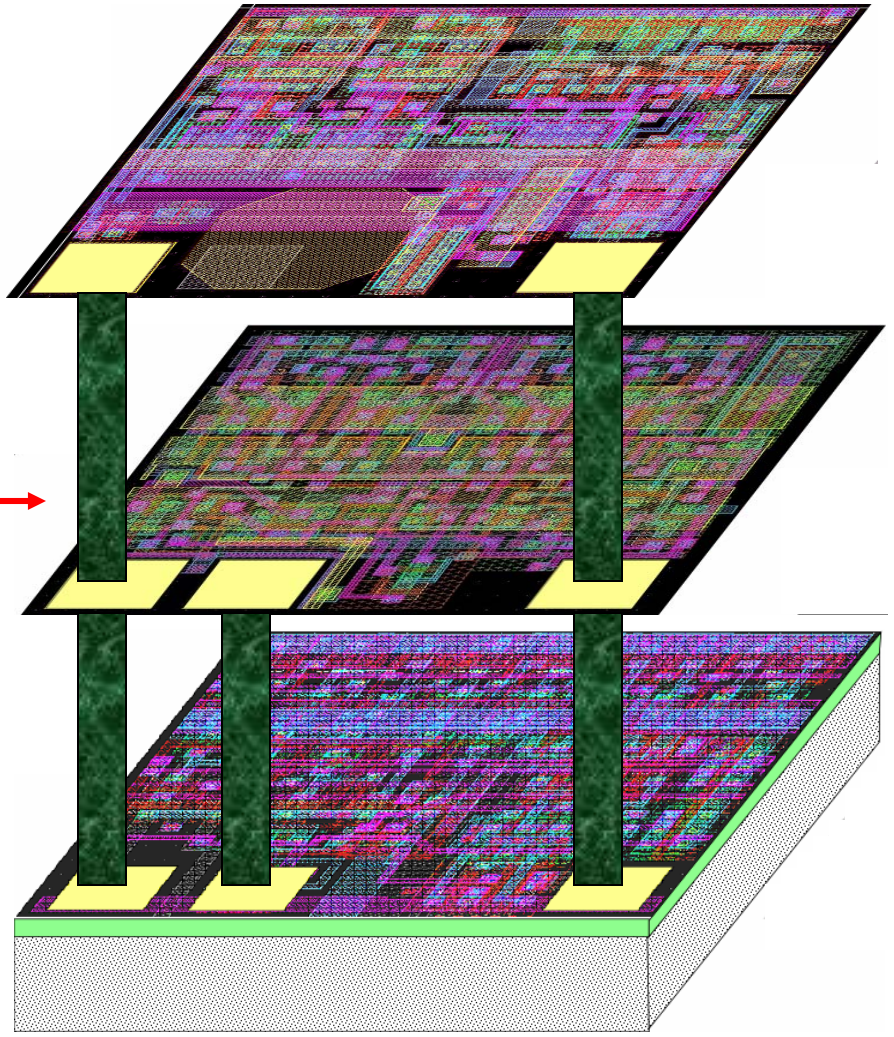
3D Stacking with Vias (step 4)

Bond tier 3 to tier 2



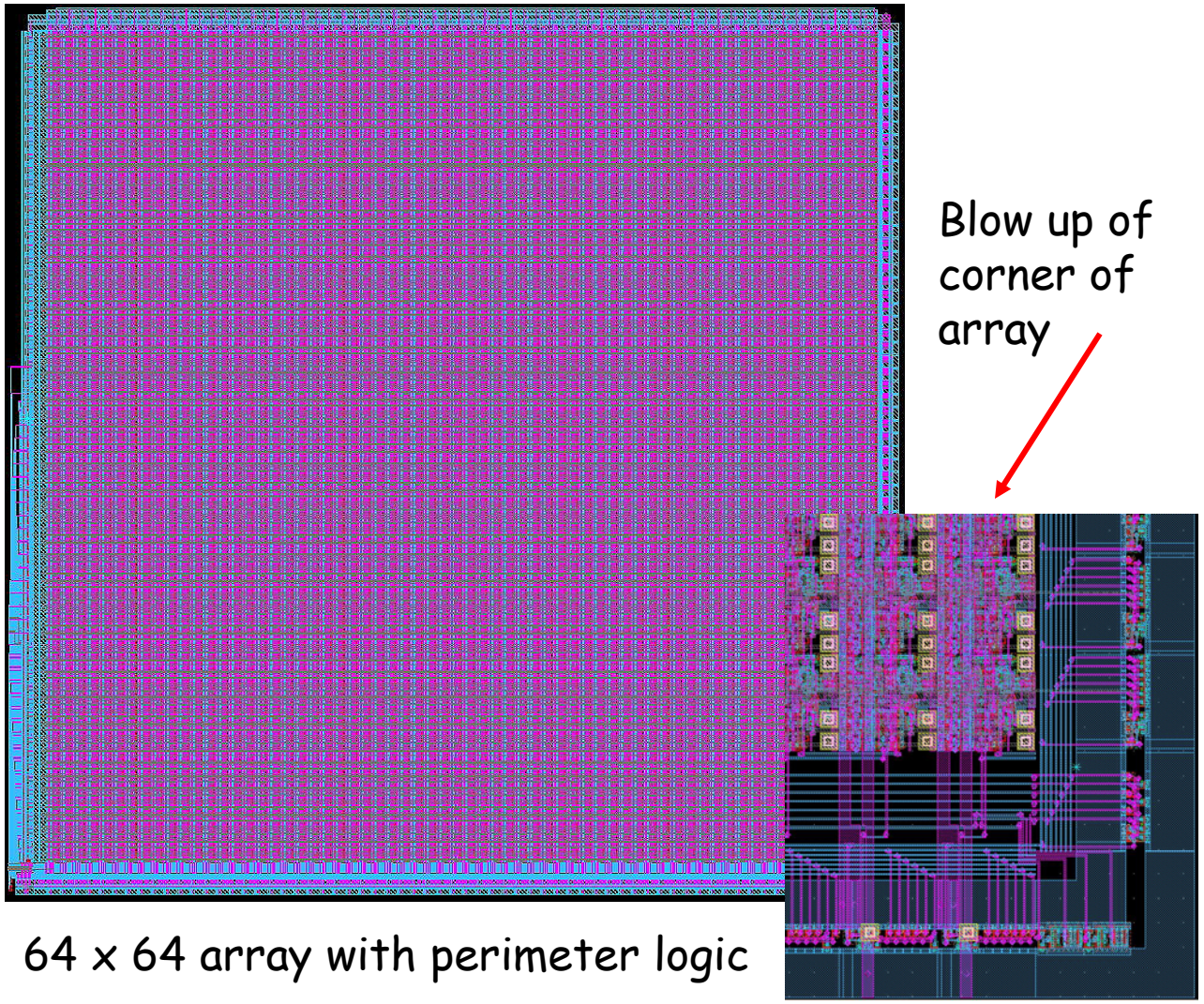
3D Stacking with Vias (step 5)

Form 2 vias, 1.5 x 7.3 μm, through tier 3 to tier 2



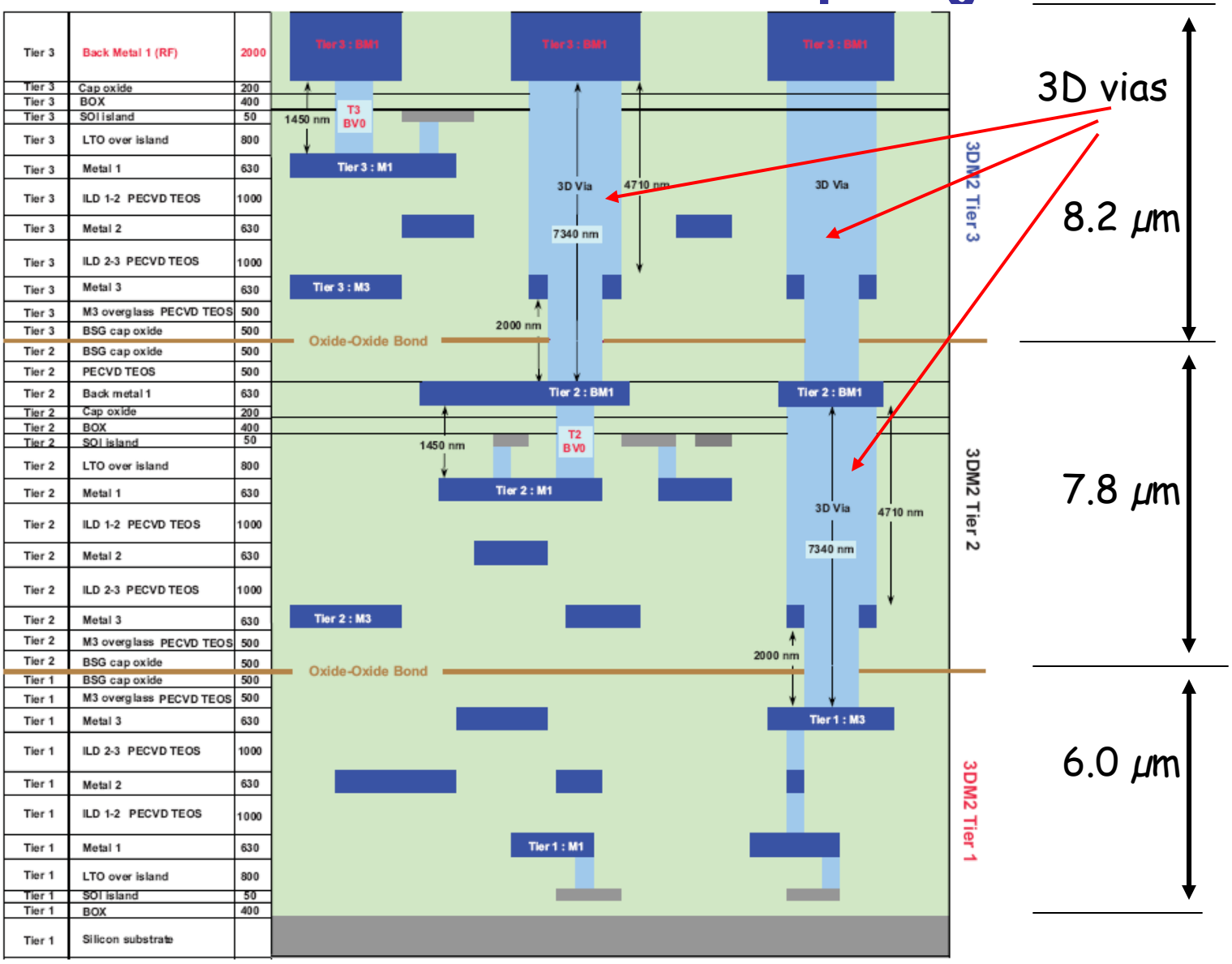
Perimeter Logic

- Perimeter circuitry for the ILC Demonstrator chip occupies a small amount of space.
- Area for the perimeter logic could be reduced in future designs.



64 x 64 array with perimeter logic

MIT LL 3D Multiproject Run



Demonstrator Chip Summary

- Multi functional device to be used a proof of concept
- 64 x 64 array that can be expanded to 1000 x 1000.
- 175 transistors in 20 micron pixels
- 3 tiers of transistors with an active circuit thickness of 22 microns
- Pulse height information (analog output) may not be required in the final design
- Sparsification with look ahead skip speed of 200 ps/cell for token passing.
- Two types of time stamping (only one chosen for the final application). 32 time stamps available, can be expanded to 64.
- Test input for every cell. Can be expanded to include a disable for every cell with little or no increase in size.

Demonstrator Chip Summary (con't)

- Serial digital output on one line
- Small peripheral circuitry.
- Chip power dissipation set by analog needs
  - Analog power = 0.75 μw/pixel => 1875 $\mu w/mm^2$
  - For ILC vertex detector power should not exceed 20 $\mu w/mm^2$
  - The vertex detector is expected is expected to acquire data for 1 msec every 200 msec
  - Assuming the analog power is ramped up in 0.5 msec, is held for 1 msec and ramped down in 0.5 msec the analog power for the ILC demonstrator chip would be 18.75 $\mu w/mm^2$
- Noise is expected to be in the range of 20-30 e- when connected to the detector.
- Multi-project submission date October 1

3D IC Advantages

- Increased circuit density without going to smaller feature sizes
  - ILC demonstrator has 175 transistors in a 20 μm pixel
- Unlimited use of PMOS and NMOS transistors
- 100% diode fill factor
- SOI Advantages
  - High resistivity substrate for diodes provide large signals
  - Minimum charge spreading with fully depleted substrate
  - Inherently isolated vias
- 3D may be used to add layers above other sensors types currently under development.

Some 3D IC Design Challenges

- Cross talk between devices on different levels.
- Placement and reducing the number of vias.
- Power distribution.
- Working with new technologies

Conclusion

- Industry is moving toward 3D integrated circuits.
- 3D is a natural progression for higher performance and higher functionality.
- 3D is opening new approaches for HEP
  - Pixels arrays is one example
- Several approaches are possible for pixels
  - Die to wafer bonding
  - Wafer to wafer bonding
  - A combination of the above
- Fermilab is working on several approaches to 3D integration

Acknowledgements

- I would like to acknowledge the work done by the designers of the 3D demonstrator chip who completed the entire design in only 3 months
  - Gregory Deptuch, BNL
  - Jim Hoff, FNAL
  - Tom Zimmerman, FNAL
- I wish to thank the ILC design group at Fermilab for their helpful comments.

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