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# Monolithic CMOS Pixel Sensors for High Resolution Particle Tracking

## Outlook

- Principle of CMOS MAPS
- Device simulation
- Example of prototypes designed at LEPSI
- Beam test results
- Radiation hardness tests
- Some future application (particle tracking and radiation imaging)

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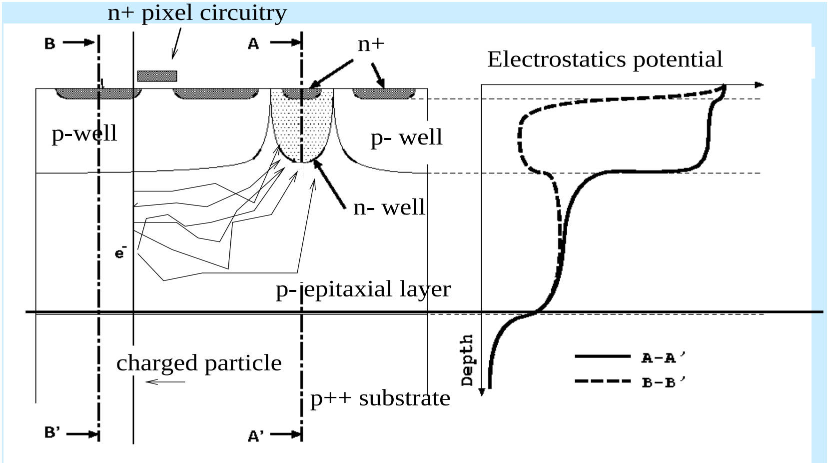
# Monolithic Pixel CMOS Sensor for Particle Tracking

## From digital still and video cameras to particle tracking device

Twin - tub (double well), CMOS process with epitaxial layer




- The effective charge collection is achieved through the thermal diffusion mechanism,
- The device can be fabricated using a standard, cost-effective and easily available CMOS process,
- The charge generated by the impinging particle is collected by the n-well/p-epi diode, created by the floating n-well implantation,
- The active volume is underneath the readout electronics allowing a 100% fill factor.

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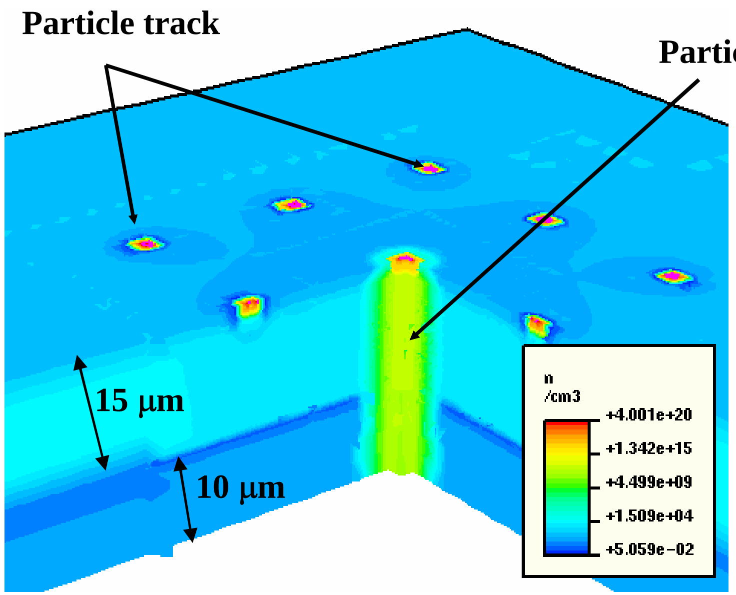
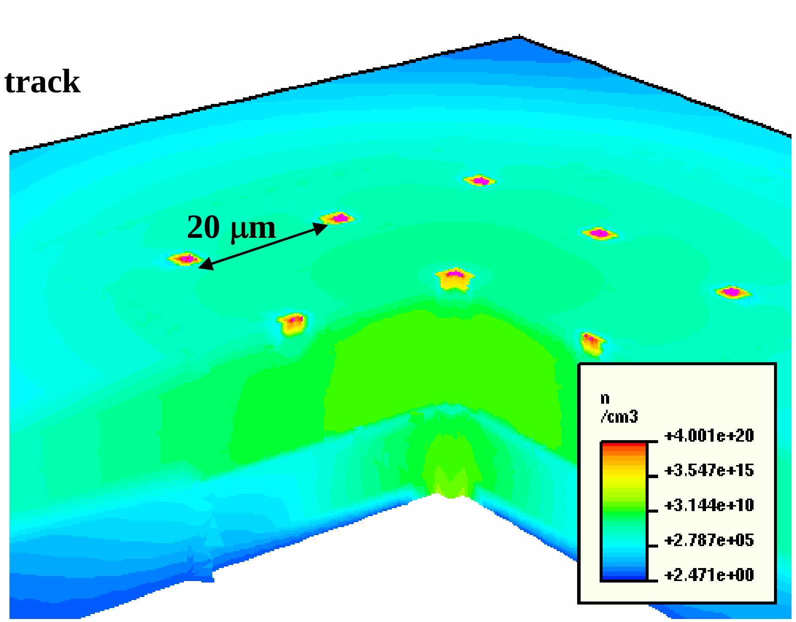
# CMOS MAPS device simulations using ISE-TCAD

## ☑ Simulation of physics process




**$\tau$ = 0 ns** **Carrier concentration** **$\tau$ = 25 ns**

- The charge collection efficiency examined using the mixed mode device and circuit simulator DESSIS-ISE from the ISE-TCAD package,
- The charge collection is traced as a relaxation process of achieving the equilibrium state after introducing an excess charge emulating passage of the ionising particle
- The device is described in three dimensions by a mesh generated using the analytical description of doping profiles and the boundary definition corresponding to the real device,
- Different detector parameters, including the thickness of the epitaxial layer, the size of a pixel and collecting diodes and number of diodes per pixel, were investigated.

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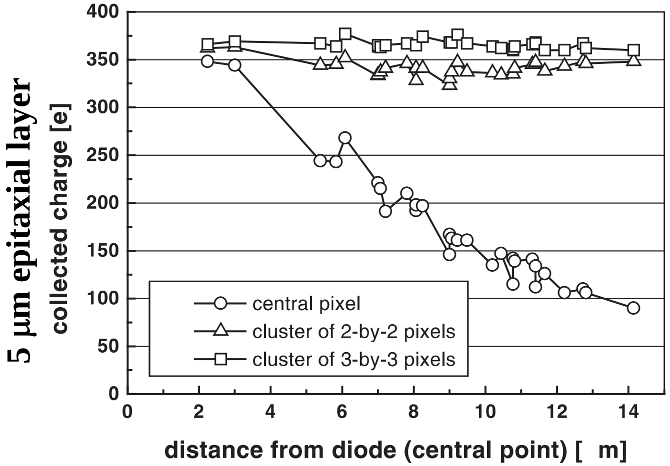
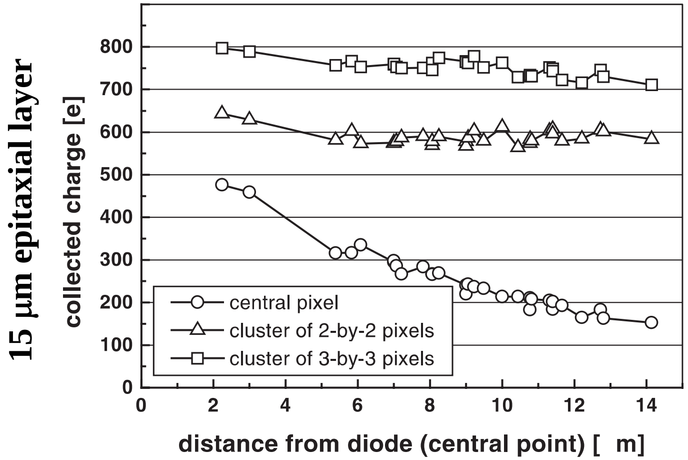
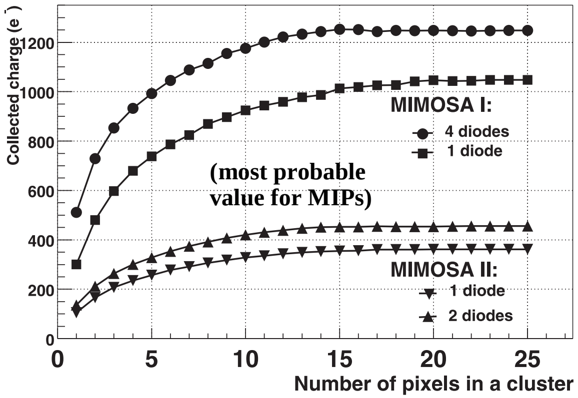
# Device simulations results and measurements on prototype

## ☑ Simulation of physics process

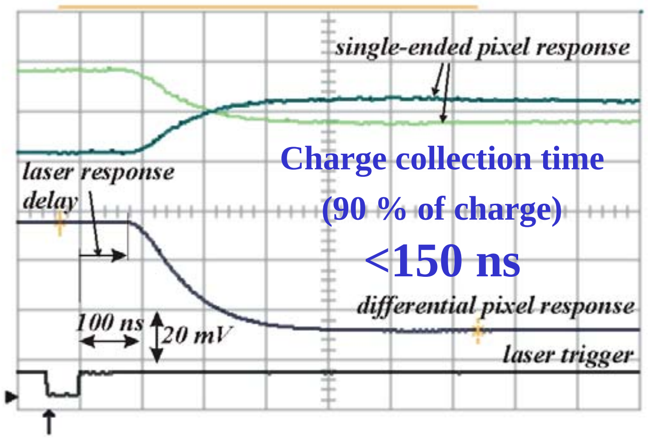



- **Experimental verification:**




The measured collected charge for two chips having 14 µm and less then 5 µm, the pitch of 20 µm



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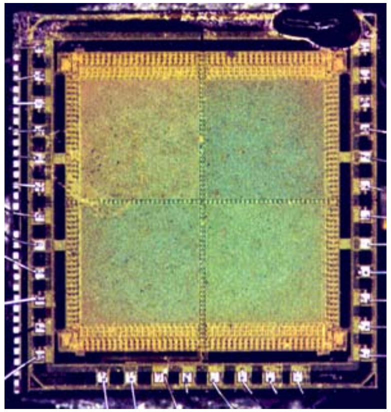
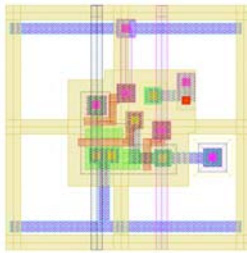
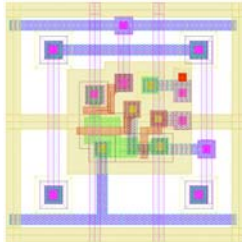
# MAPS prototypes at LEPSI

☑ **Prototype chips - MIMOSA I** ***(MinimumIonising Particle MOS Active Pixel Sensor)***



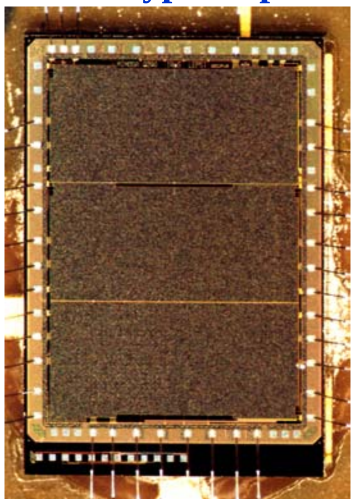
**die size 3.6x4.2 mm$^2$**





- **0.6 μm CMOS ($t_{ox}$=12.7 nm)**
- **14 μm thick EPI layer ($10^{14}$ cm$^{-3}$)**
- **4 arrays 64x64 pixels, pitch 20x20 μm$^2$**
- **diode (nwell/p-epi) size 3x3 μm$^2$ - 3.1 fF**

☑ **Prototype chips - MIMOSA II**



**die size 4.9x3.5 mm$^2$**

- **0.35 μm CMOS ($t_{ox}$=7.4 nm)**
- **4.2 μm thick EPI layer ($10^{15}$ cm$^{-3}$)**
- **6 arrays 64x64 pixels, pitch 20x20 μm$^2$**
- **diode (nwell/p-epi) size 1.7x1.7 μm$^2$ - 1.65 fF**
- **radiation tolerant transistor design**

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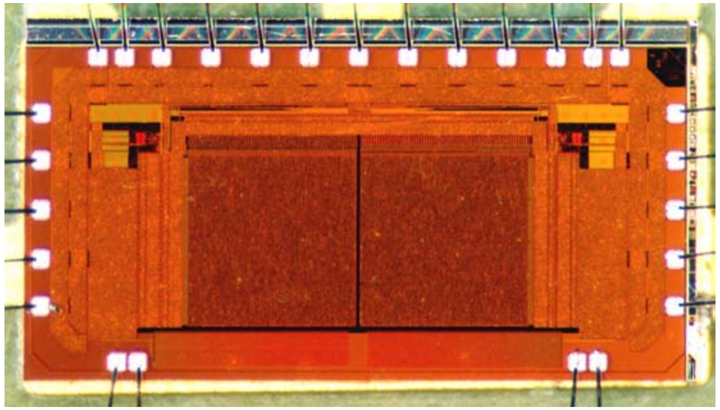
# MAPS prototypes at LEPSI

## ☑ Prototype chips MIMOSA III

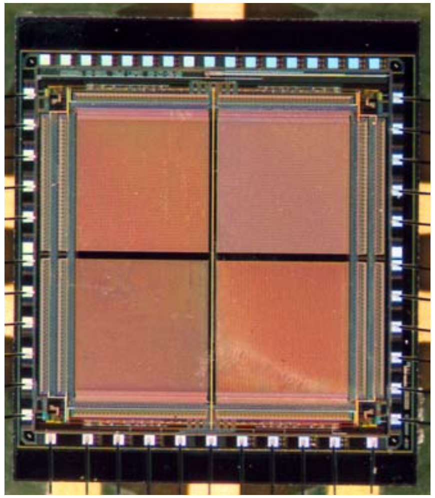
- **Collaboration with Microelectronics Group of CERN - MIMOSA III**



- **standard 0.25 μm CMOS (tox=5.84 nm)**
- **2 μm thick EPI layer (~$10^{15}$ $cm^{-3}$)**
- **2 arrays 128x128 pixels, pitch 8x8 $\mu m^2$**
- **diode (nwell/p-epi) size 1x1 $\mu m^2$ - 2.1 fF**
- **radiation tolerant transistor design**
- **optimisation for low noise ~6 $e^-$ @ 20MHz**

**die size 4.0x2.0 $mm^2$**

## ☑ Prototype chips - MIMOSA IV



- **0.35 μm CMOS (tox=7.5 nm)**
- **p-substrate process (~$10^{14}$ $cm^{-3}$)**
- **4 arrays 64x64 pixels, pitch 20x20 $\mu m^2$**
- **diode (nwell/p-epi) size 2x2 $\mu m^2$ - 1.8 fF**
- **radiation tolerant transistor design**
- **charge collection from non epitaxial substrate**
- **new structures of charge sensing elements:**
  - **charge spill-gate,**
  - **current mode pixel,**
  - **self-biasing diodes**

**die size 3.7x3.8 $mm^2$**

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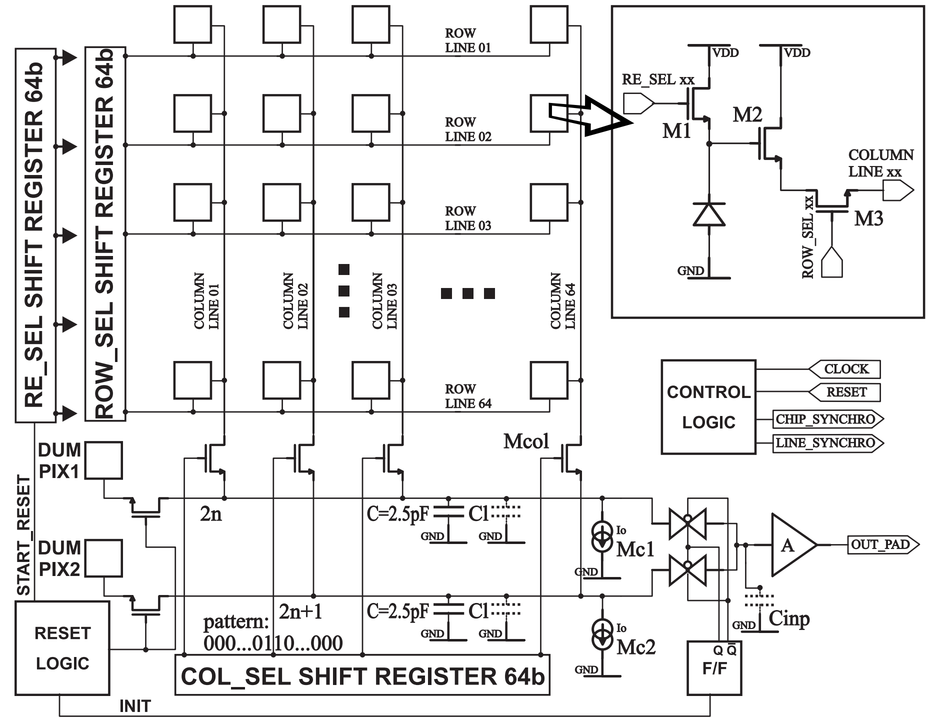
# Double Correlated Sampling: readout scheme

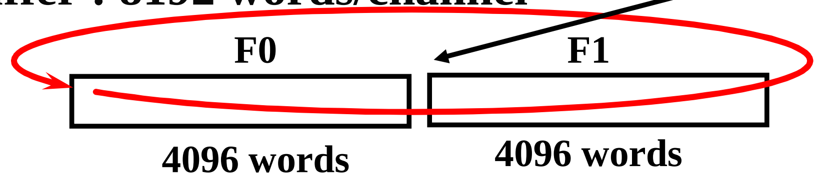
☑ **Present readout and data processing**




**Fast ADC 12 bits**

**Buffer : 8192 words/channel**

trigger !



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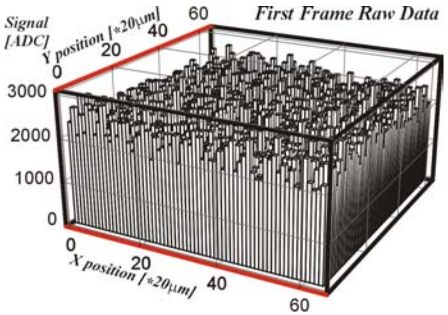
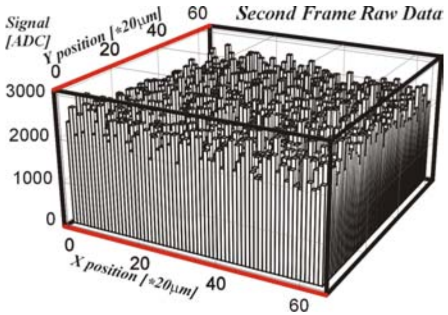
# Double Correlated Sampling: data processing

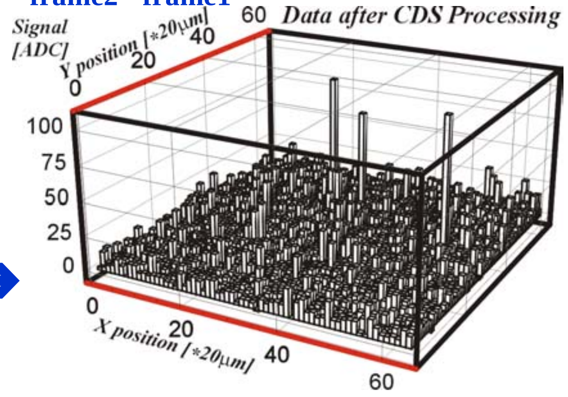
## ☑ Present readout and data processing

- Off-line CDS:

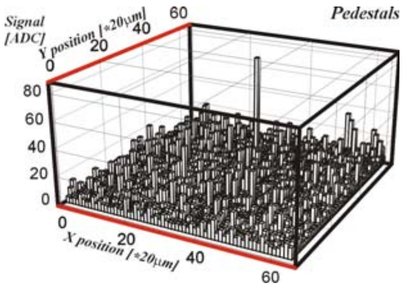


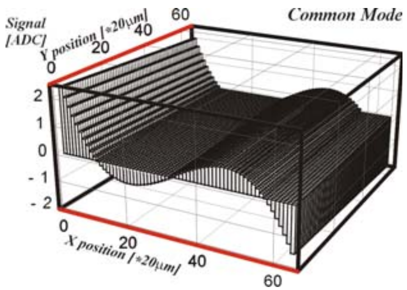

frame2 - frame1

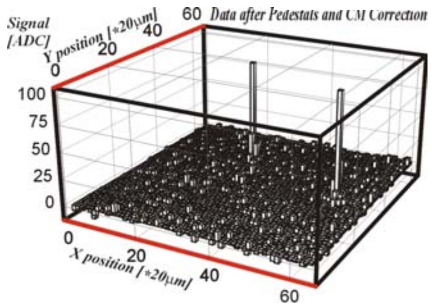



- CDS Pedestals:

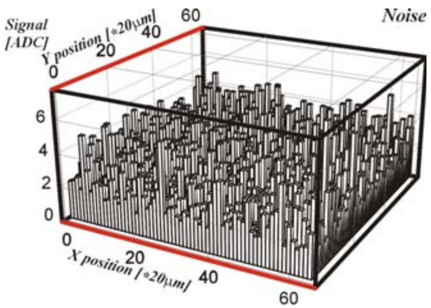


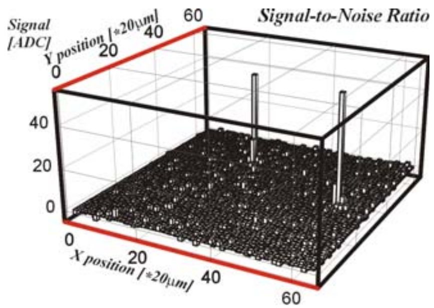

- Common Mode:




- Temporal noise distribution:




- Signal-to-noise ratio evaluated for considered event

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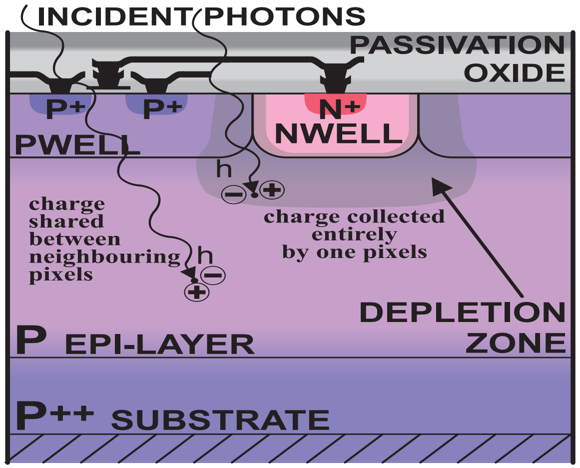
# MAPS calibration using X-ray source

## ☑ Calibration of the conversion gain - with soft X-rays

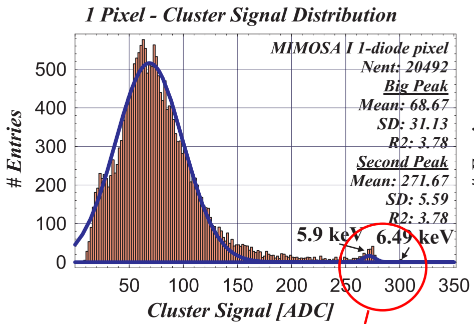
- Calibration methods:

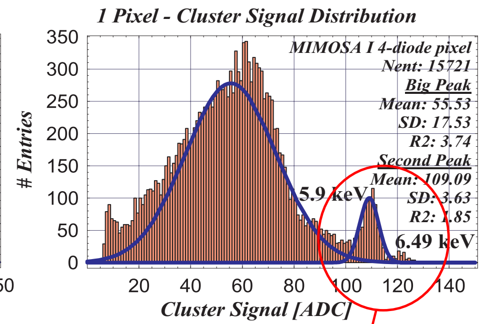
**Emission spectra of a low energy X-ray source e.g. iron $^{55}Fe$ emitting 5.9 keV photons.**

*very high detection efficiency even for thin detection volumes - $\mu$ =140 cm$^2$/g, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon*



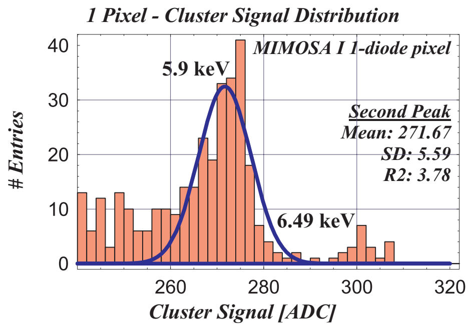

The ' warmest ' colour represents the lowest potential in the device

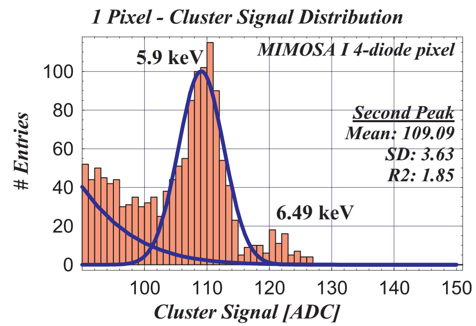



**MIMOSA I (14 µm EPI) configuration with single diode in one pixel**

**MIMOSA I (14 µm EPI) configuration with four diodes in one pixel**




| | | |
|---|---|---|
| MIMOSA I CMOS 0.6 µm | 1 diode – 14.6 µV/e$^-$ | 4 diode – 6.0 µV/e$^-$ |
| | ENC = 14 e$^-$ @1.6 ms f. rate | ENC = 30 e$^-$ @1.6 ms f. rate |
| MIMOSA II CMOS 0.35 µm | 1 diode rad. tol.– 22.9 µV/e$^-$ | 2 diode rad. tol.– 17.5 µV/e$^-$ |
| | ENC = 12 e$^-$ @0.8 ms f. rate | ENC = 14 e$^-$ @0.8 ms f. rate |

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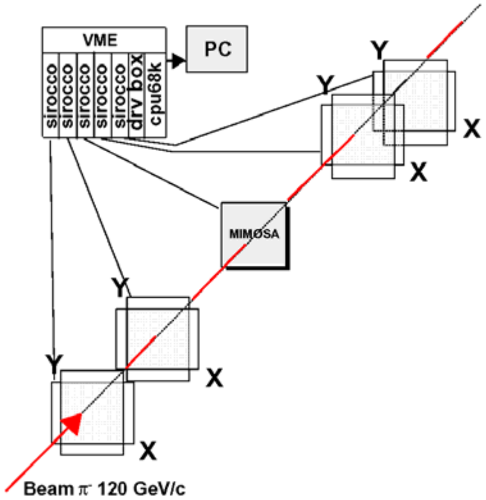
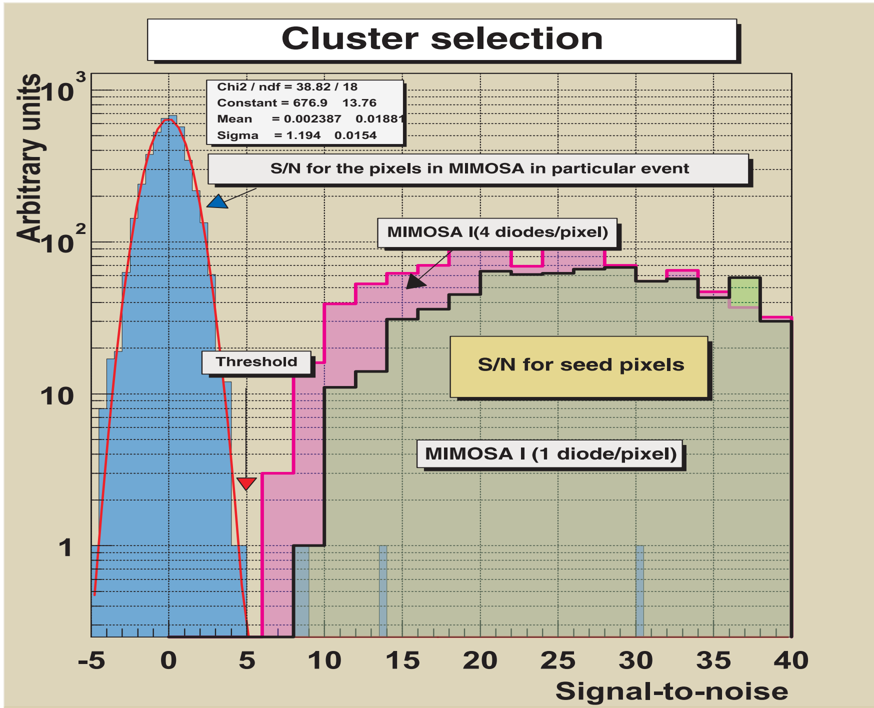
# CMOS Monolithic Pixel Sensor: MIP tracking tests

☑Beam tests results




… the track position in the middle of the telescope is predicted with the precision of **~1 µm**

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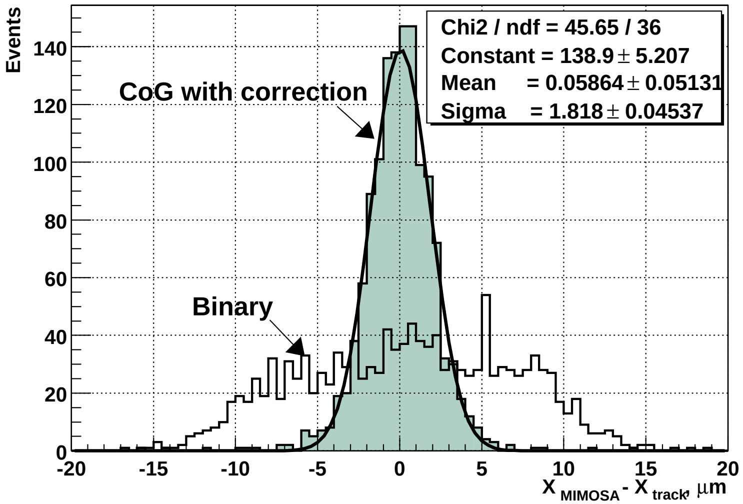
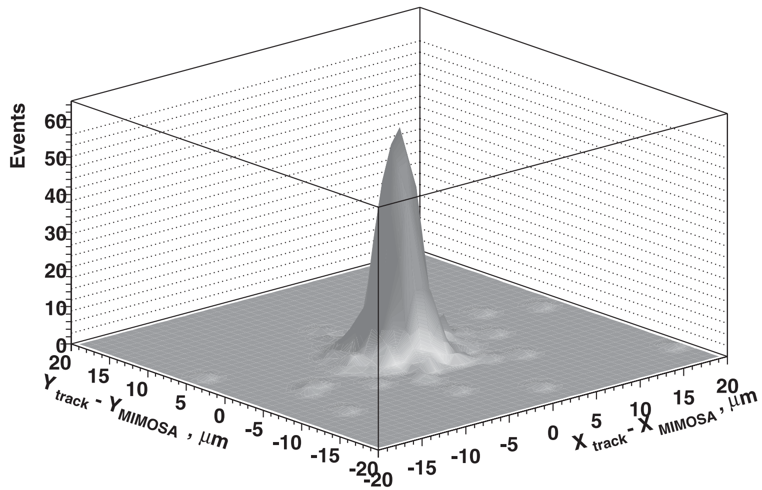
# CMOS Monolithic Pixel Sensor: tracking performance




**ENC<10 electrons**
**S/N>30**

**Efficiency (5σ S/N seed cut):**
$\varepsilon_{\text{hits} < 20\ \mu\text{m}} = 99.5\ \%$

**Spatial resolution:**
$\sigma = 1.4\ \mu\text{m}$

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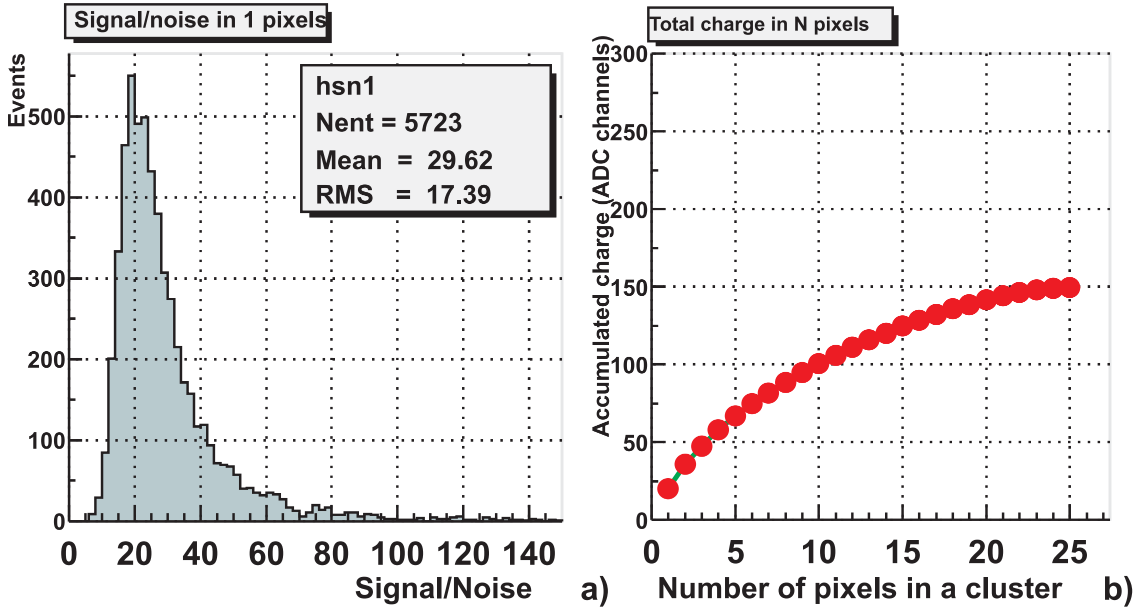
# MIMOSA-4 (no-epi substrate) test results:

**0.35 mm AMS process <u>without epitaxial layer</u>**
**but with low doping (resistivity) substrate**




## Observed performances with 120 GeV/c p- at CERN-SPS:

- Detection efficiency ~99.7%
- S/N ~30 but charge is wider spread
- Spatial resolution ~4 μm (20 μm pitch)

**Technology without epitaxial layer seems worth investigating and optimizing**

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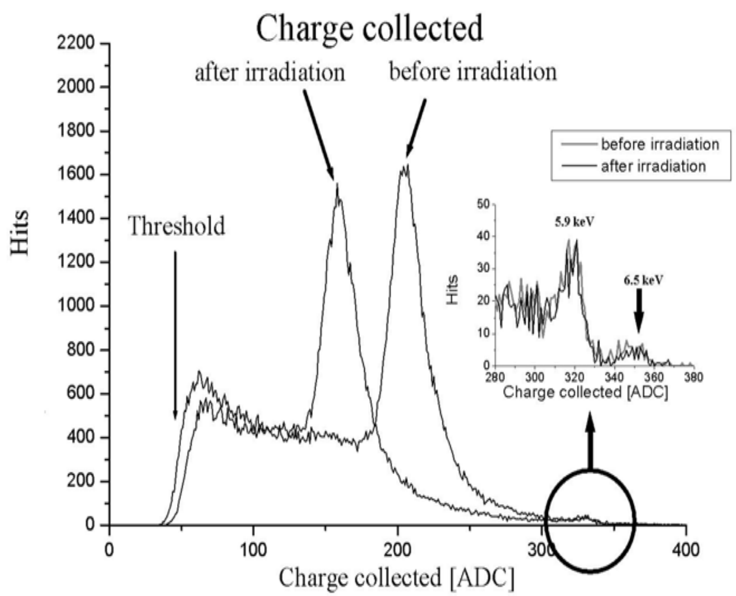
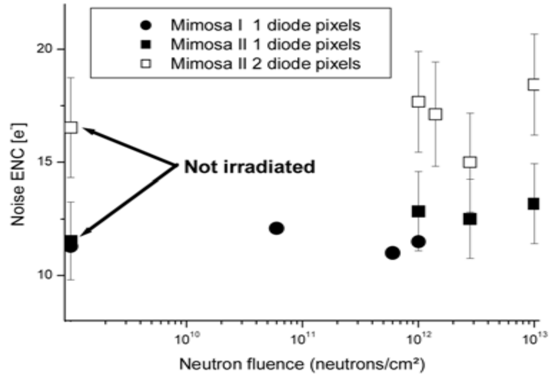
# Neutron radiation tolerance

Chips irradiated with neutron sources at JINR and CEA-Saclay reactors were tested with $Fe^{55}$ X-ray source.

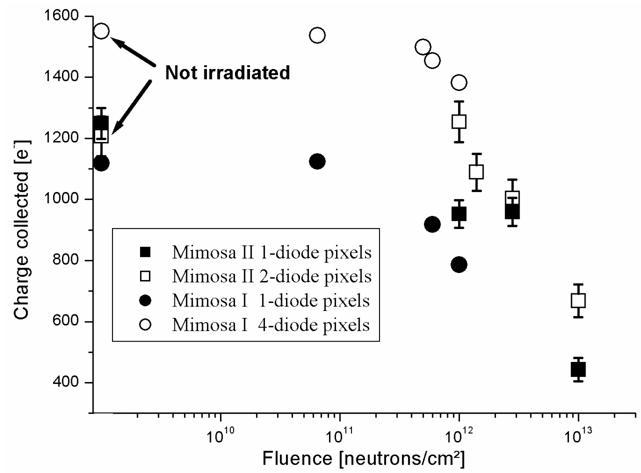



**Charge loss is observed only for fluences $>10^{11}$ n/cm$^2$ what is 2 orders of magnitude more than it is expected for TESLA!**

## Noise as a function of fluence:




## Observed charge loss as a function of fluence:



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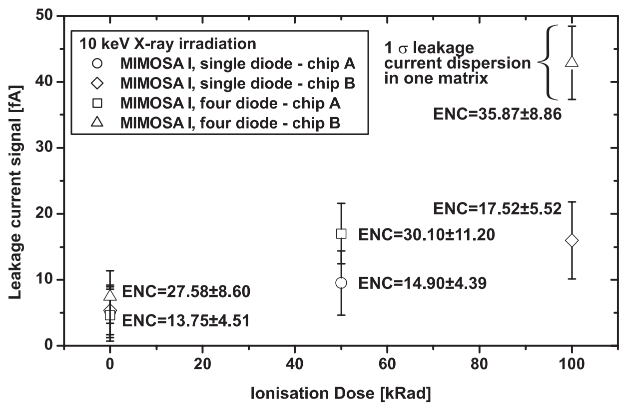
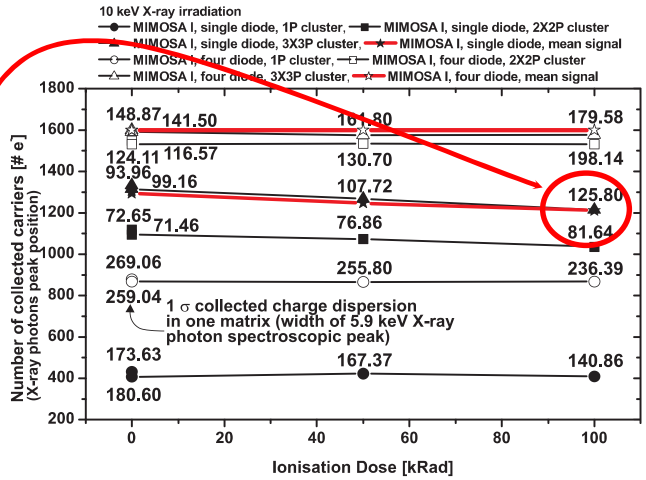
# Ionizing radiation tolerance

## Irradiation damages are results of charge built-up in isolation material - oxide

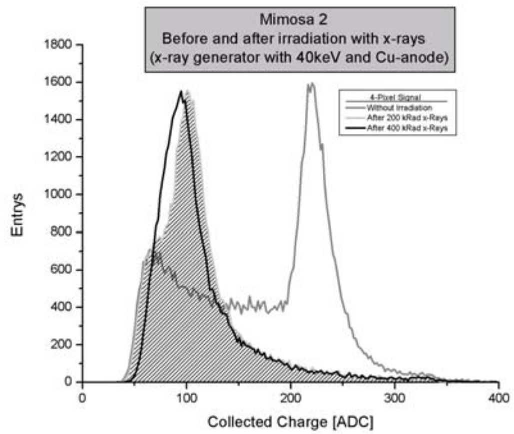
MIMOSA I increase of leakage current



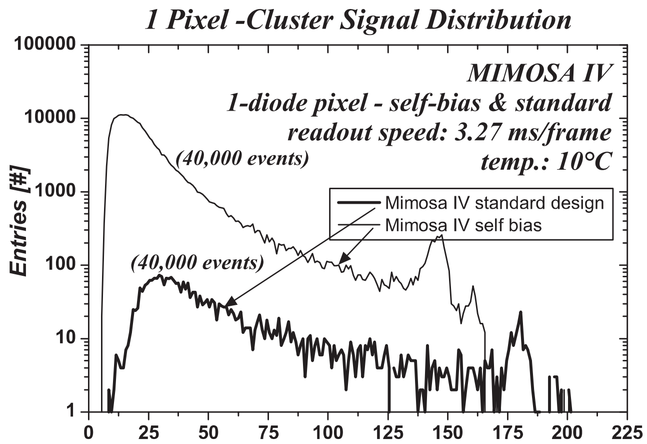

MIMOSA I slight losses in collected charge




MIMOSA II strong charge losses in collected charge




MIMOSA IV - non irradiated shows dependence of charge collection on pixel layout: this has effect like irradiation!




**Understanding not clear at all - much more studies needed...**

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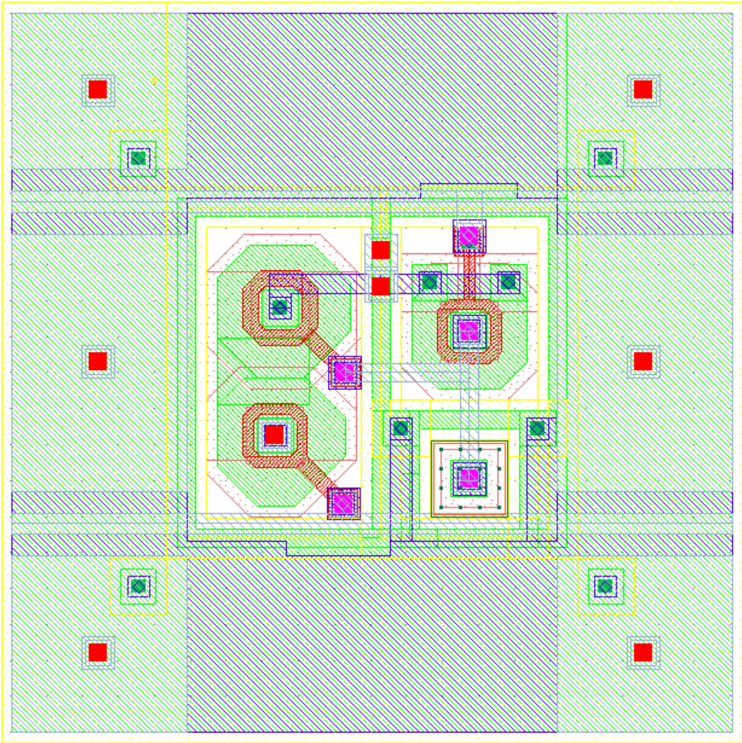
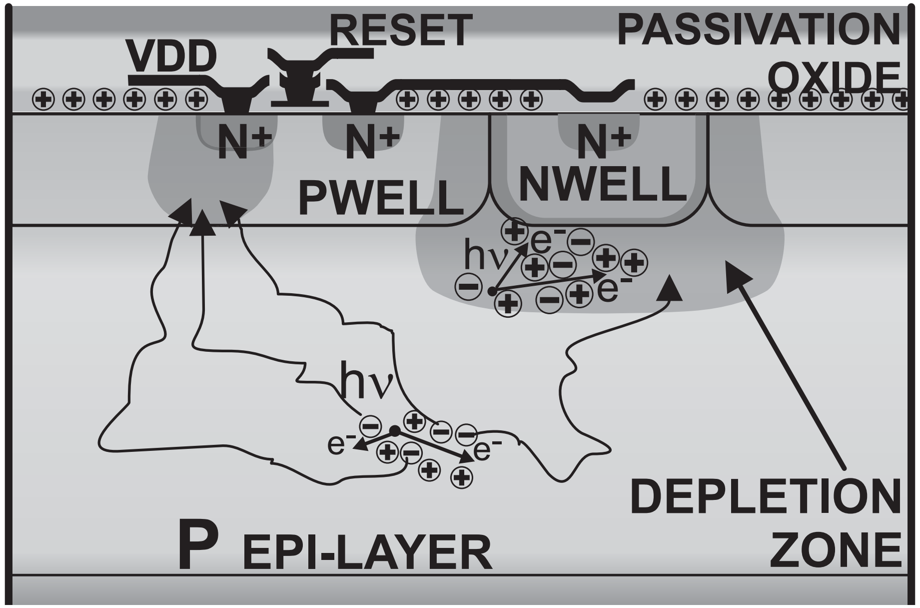
# Working hypothesis to explain Mimosa4 case

MIMOSA IV
pixel layout suffering from
poor charge collection






Competitive charge collection path
to the reset transistor node,
through "transparent" P-well

**In order to understand (and simulate) this effect, much more precise data on doping profile are needed!**
**Technology test structure needed!**

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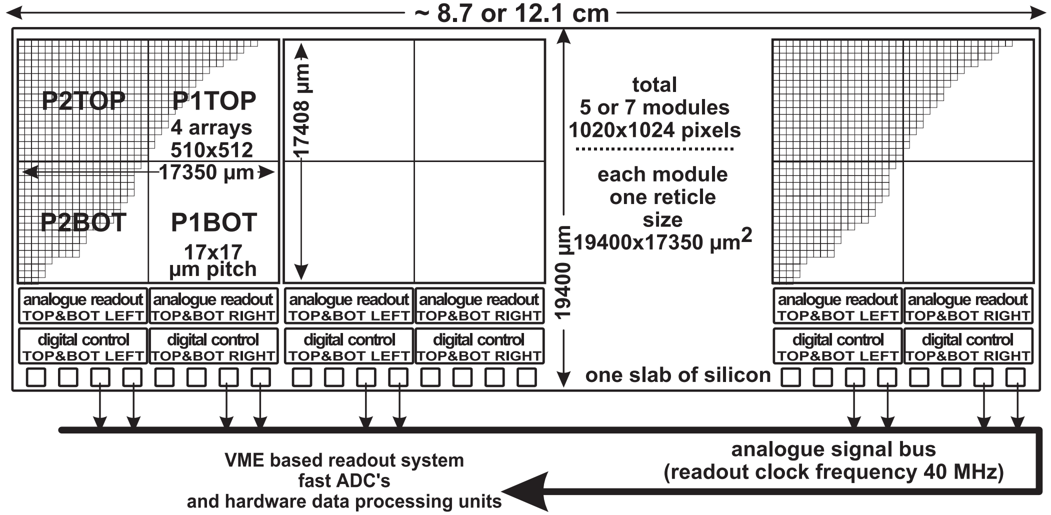
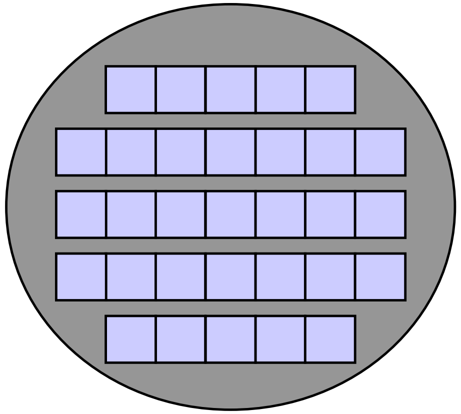
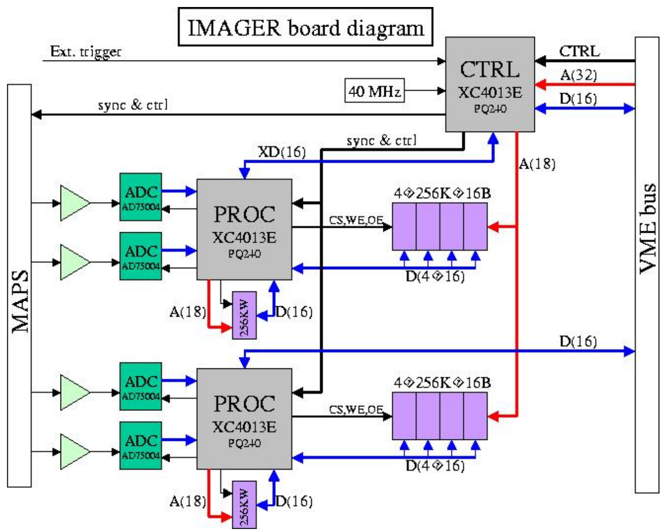
# MAPS wafer scale prototype: Mimosa 5

## ☑ MIMOSA V - wafer scale detector



- ☑ stitching: coarse - 100 µm + scribeline, option:precise - 1 µm
- ☑ normal readout: 6ms/frame, fast sampling readout: 100 µs/frame
- ☑ 0.6 µm with 14 µm epitaxial layer
- ☑ lot of six 6’’ wafers 44 kEuro
- ☑ analogue readout - with hardware processing
- ☑ acquisition board with hardware processor - pedestal subtraction, CDS, S/N analysis, sparsification on-line.



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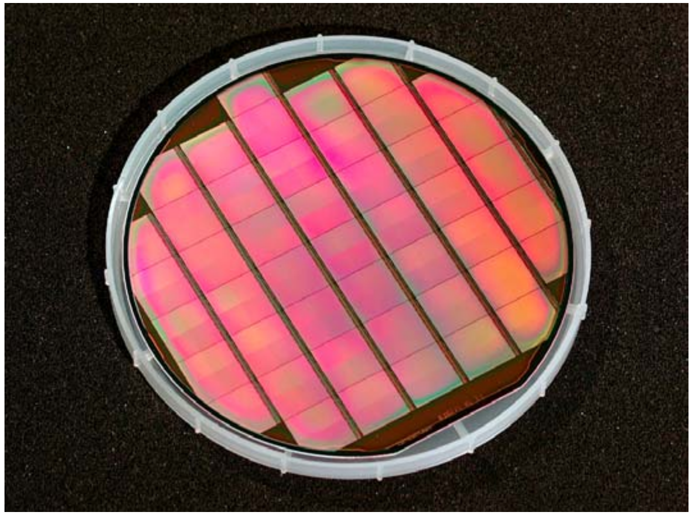
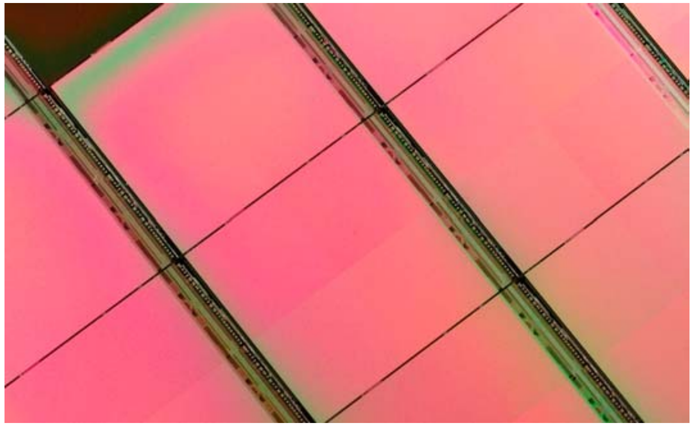
# MAPS wafer scale prototype: Mimosa 5





**Mimosa-5 status**

- **6 wafers delivered by AMS**
- **3 wafer back-thinned (down to 120μm) and sliced**
- **prober tests of all wafers in progress: first estimation of yield ~30%**
- **beam tests at CERN: results as expected**
- **fine back-thinning tests at CNM Barcelona and ITE Warsow**

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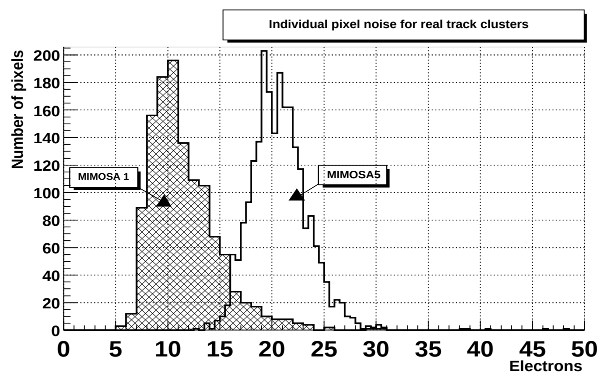
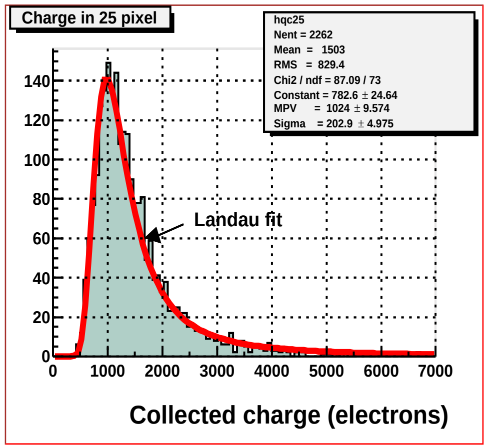
# MIMOSA-5 tests

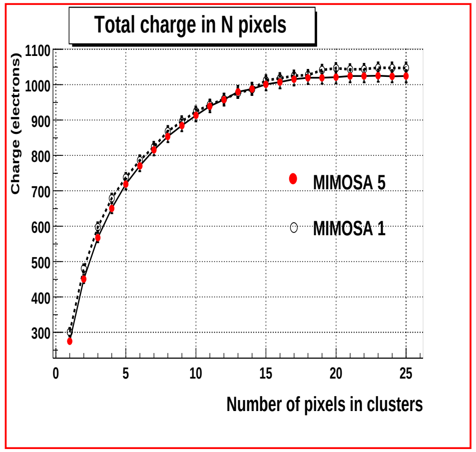
**The chip (4 matrices of 512×512 pixels (17x17 μm² )**
**0.6 μm AMS process, etched down to 120 μm**
**exposed to 120 GeV/c $\pi^-$ beam at CERN-SPS**

**The same process as MIMOSA-1 ⇨ the same performances expected?**

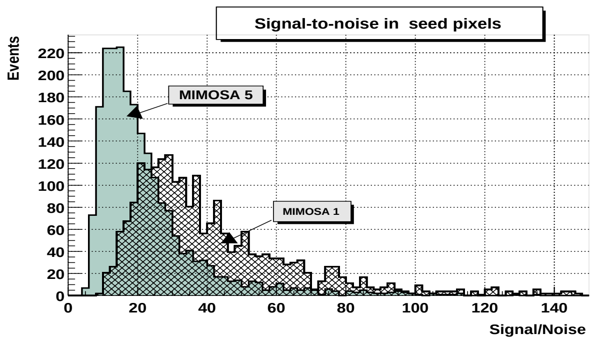
**Larger noise relative to M1 (different serial r.o.architecture)**




**Epitaxy layer ~14 mm ⇨ charge ~1000$e^-$**




**Preliminary results:**
**$\varepsilon$ ~99.3%,**
**$\sigma_{sp}$ ~1.7μm,**
**$\sigma_{gain} \leq$ 2-3%**

**close to those of MIMOSA-1**

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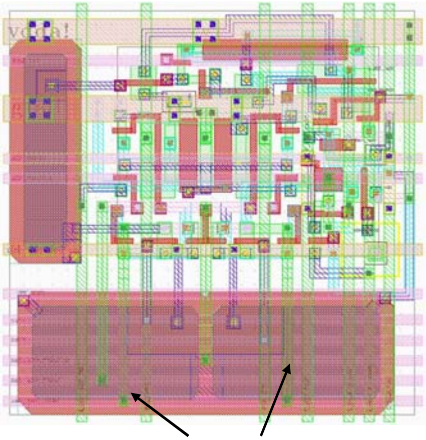
# MIMOSA-6 – first sensor with integrated functionality

**0.35 MIETEC technology (same as MIMOSA-2)**
**IReS-LEPSI/DAPNIA collaboration**

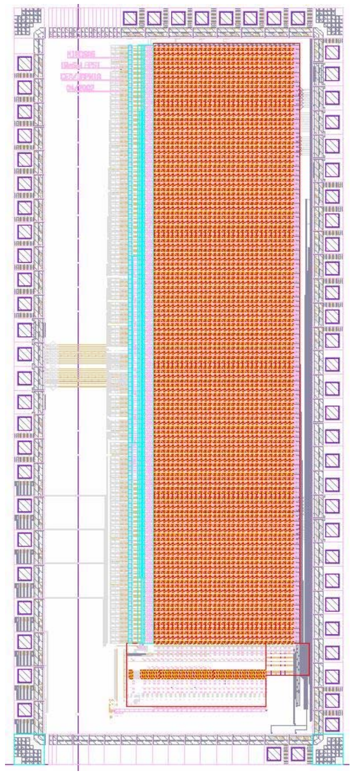
- **24 column readout in parallel**
- **128 pixels per column**
- **5MHz effective readout frequency**
- **Amplification (x5.5), Correlated Double Sampling on pixel**
- **Discriminator integrated on chip periphery (1 per column)**
- **Power dissipation ~500 μW per column**



Charge storage capacitors

**Pixel layout:**
**28x28 $\mu m^2$**

29 transitstors



**Chips are back from foundry and under tests.**
**First results quite promising.**

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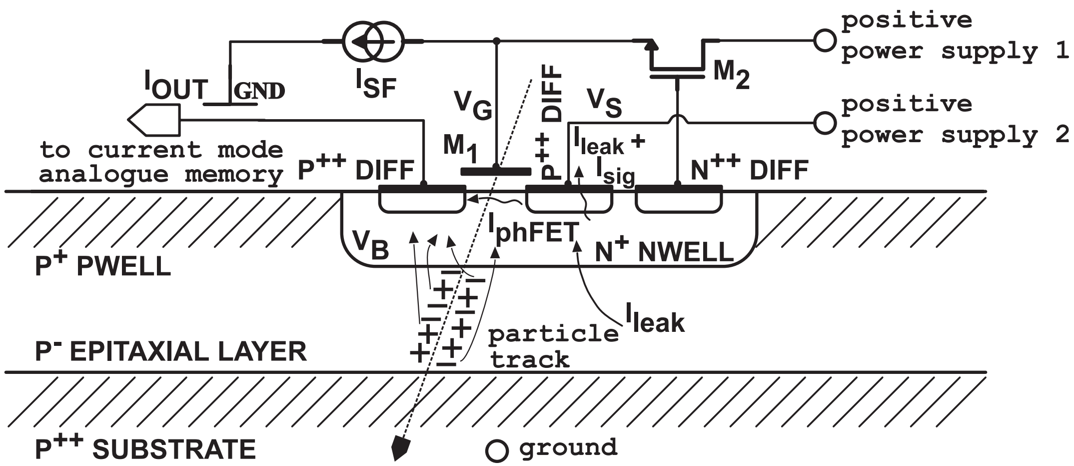
# Future development example: FotoFet




**First results very promising (e.g. ENC ~4 electrons)!**

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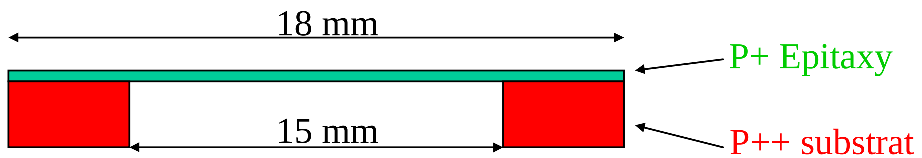
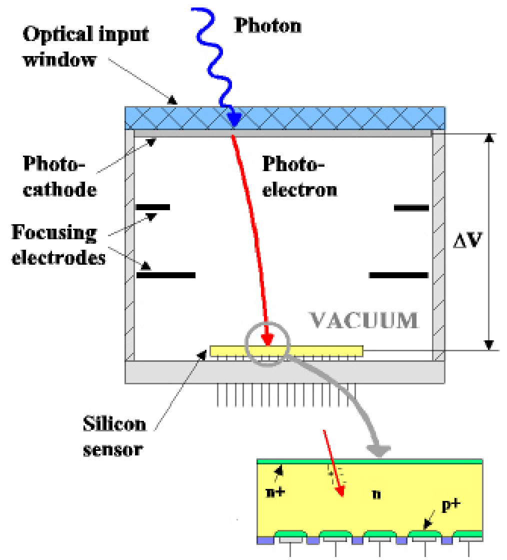
# Monolithic CMOS Pixel Detectors for Radiation Imaging? A lot still to be done!

1. Visible light: first and the most important commercial application!
2. X and γ imaging: not very appropriate (except dental imagers using scintillating converter)
3. α and electron (β) imaging/dosimetry
4. Neutron imaging (using Be or Ga converter foils)




**Back - thinning for low energy electrons imaging**




**Hybrid Photo Diode (HPD) ---> single photon imaging**

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# Conclusions

☑ **Good performance of CMOS pixels successfully demonstrated with small scale prototypes ε~99%, S/N~20-40, σ~1.5-2.5 μm @ 20x20 μm² pixels ,**

☑ **First wafer scale chip - works according to expectation!**

☑ **Access to processes with epitaxial layer (e.g. TSMC CIS 0.25 μm with 8 μm p-type epitaxial layer - optimised for CMOS imagers),**

☑ **Cost effective solution (1900 USD/ 8'' wafer ⇨ 9 USD/cm² comparable to simple strip detectors),**

☑ **directions to investigate:**

- **yield optimisation of a large size chip, thinning to 20-50 μm, on-wafer stitching,**
- **data processing on-a-chip,**
- **radiation hardness understanding/improvement**
- **optimisation of the sensitive element - alternative charge sensing structures.**

☑ **R&D programme on CMOS MAPS TESLA VD in a collaboration with several other centres – aim for the detector design by 2004 -2005**

☑ **R&D program for radiation imaging application (SUCIMA, Euromedim…)**

**My acknowledgement to LEPSI and IReS teams working since 4 years on that project!**

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