Application specific architectures of CMOS Monolithic Active Pixel Sensors

M. Szelezniak on behalf of

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(*and for Mimosa VIII* - **DAPNIA**: Y. Degerli, N. Fourches, Y. Li, P. Lutz, F. Orsini**)**

***** Since March 2005 with BNL, 11973 Upton, NY, USA

OUTLINE:

- Introduction to MAPS
- Possible future applications of MAPS
  STAR VxD upgrade, ILC VxD, CBM VxD, beam monitoring (SLIM), Beta source imaging, Electron microscopy …
- MAPS based solutions for
  STAR
  ILC (outer & inner layers)
- On-pixel amplifiers
  AC & DC
- Summary

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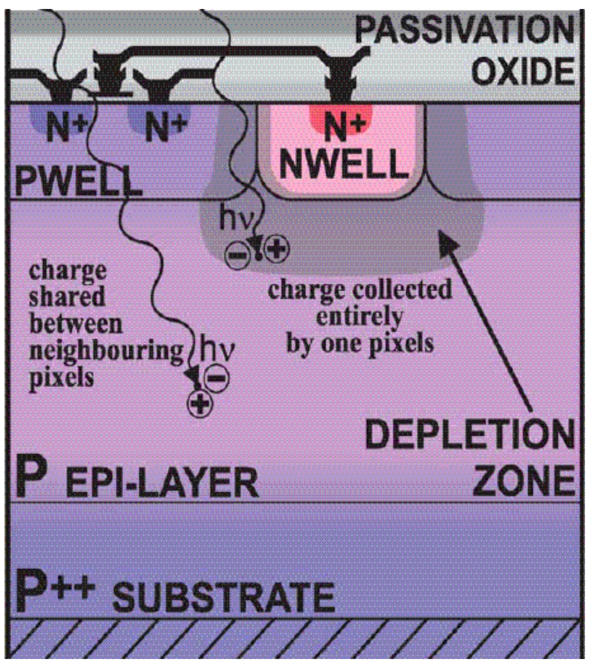
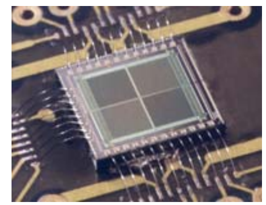
Introduction to MAPS

- The active volume is underneath the readout electronics => ~100% fill factor
- Charge generated by ionization is collected by the n-well/p-epi diode (also non-epitaxial high-res)
- Charge collection through thermal diffusion (few tens of ns)
- System on chip is possible
- No necessary post-processing (like bump-bonding)
- Thinning is possible

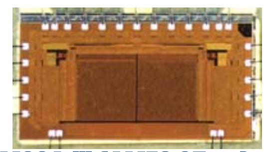


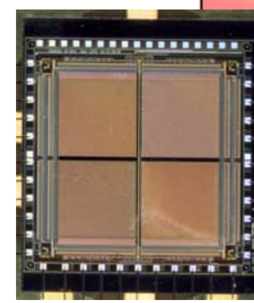
Started in 1999

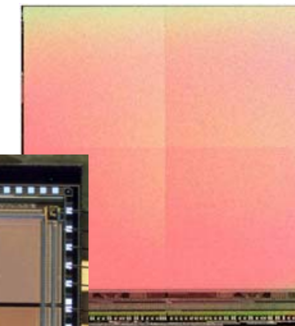
…


MIMOSA I (AMS0.6µm)


MIMOSA II (AME0.35µm)


MIMOSA III (AME0.35µm)


MIMOSA IV (AMS0.35µm)


MIMOSA V (AMS0.6µm)

By now ~15 prototypes have been fabricated and tested

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After proving the principle, it’s time to optimize MAPS for particular applications

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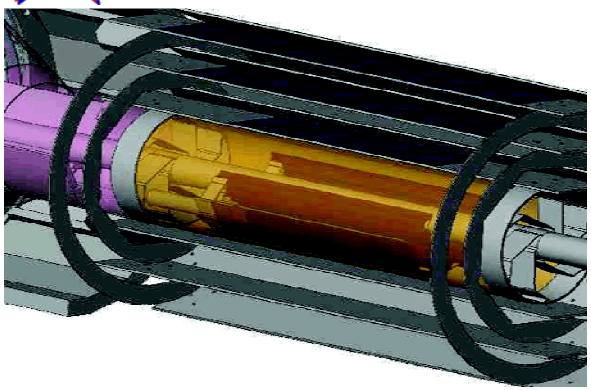
Possible applications of MAPS



STAR VxD upgrade

- readout time = integration time = 2 – 4 ms
- Room temperature operation (chip at ≲ 40°C)
- Air cooling only
- Ionizing radiation dose in 3 years ~20 krad
- Spatial resolution < 10 μm

Planned to be the first real application of MAPS

in the particle physics domain

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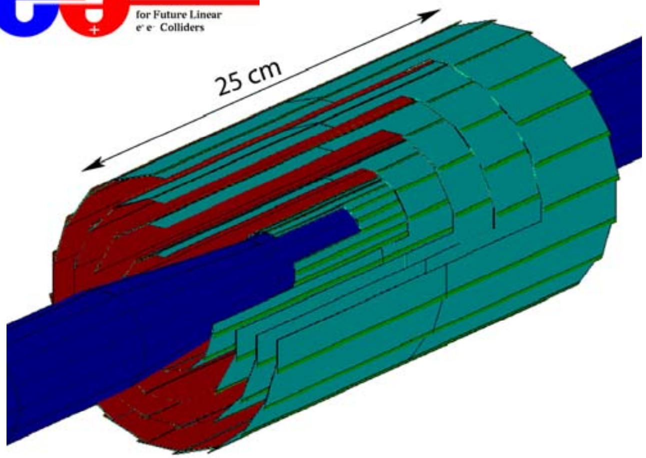
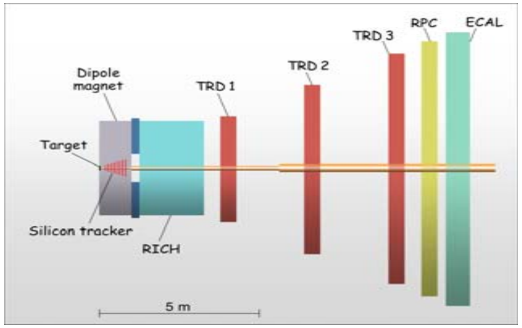
Possible applications of MAPS



ILC VxD

- •Beam train: ~1 ms every ~200 ms
- •Outer layers integration time: ≲ 200 μs
- •Inner layers integration time: ≲25 - 50 μs
- •Radiation: fluence: ≲ 10^{10} $n_{eq}/cm^2/year$
  Dose: < 50 krad/year
- •Impact Parameter < 5 μm ⊕ 10 μm /$\sin^{3/2}\theta$

see “A Vertex Detector for the ILC based on CMOS Sensors” by A. Besson @ Vertex Detectors



CBM @ GSI (Fixed Target Experiment)

see “Requirements for the Silicon Tracking System of CBM” by J. Heuser @ Vertex Detectors

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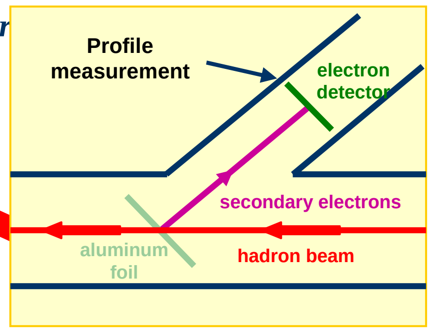
Possible applications of MAPS



On-line beam monitoring

(SLIM – SEm *(secondary emission)* for Low Interception Monitoring)

- sensitivity to 20 keV e-
- active area matrix of minimum 5000 pixels
- signal range single to 10^4 e^-/pixel every 100 μs
- 10 kHz frame rate (aiming at <2% dose non-uniformity) and no dead time
- very thin entrance window required
- CMOS sensor – thinning required

Beam profile has already been observed using final SLIM prototype and back-illuminated Mimosa V

The final chip is under tests.

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Possible applications of MAPS

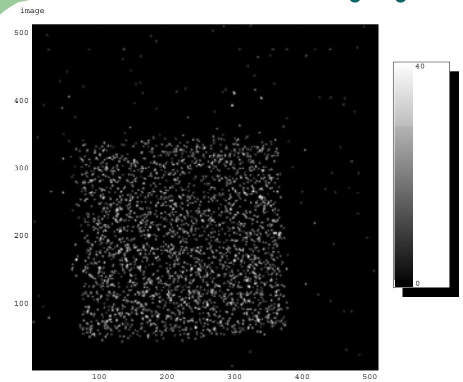

image obtained with MAPS
effective acquisition time = ~35 min

Beta source imaging: Tritium (^3H) marking

beta particles: low energy

end point energy 18.6 keV
mean decay energy 5.6 keV
most probable 3.8 keV

Mimosa V thinned down to epitaxial layer and back side illuminated proved the working principle

MAPS might be competitive to other detectors

- **high spatial resolution**
- **low cost solution**

measurements at Bonn University in collaboration with N.Wermes

Electron microscopy

Thinned **Mimosa V** with 17 µm pitch not optimized for charge sharing between pixels ⇒ resolution of **~20 lpmm**

[Measured with a scanning electron microscope (25 keV electrons)]

Requirements: radiation hardness
fast readout
resolution ≳ 40 lpmm

measurements at BNL in collaboration with P. Rehak, J. Wall

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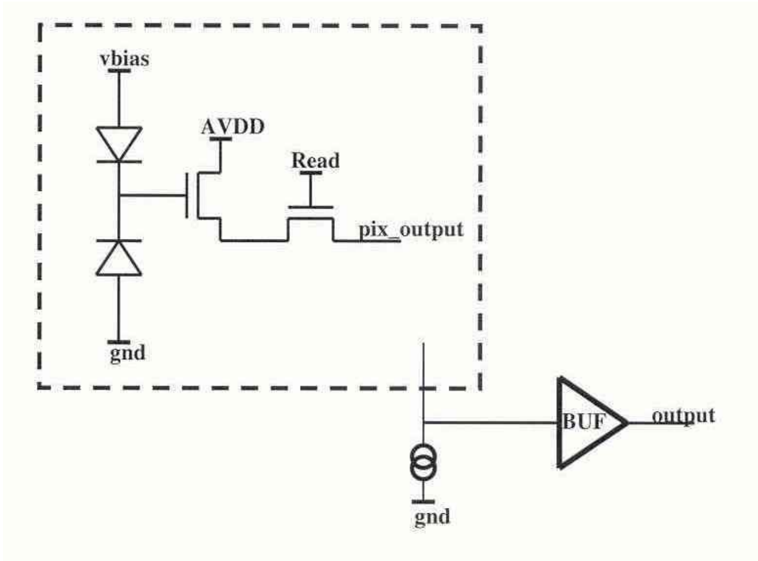
MAPS based solutions for STAR upg.

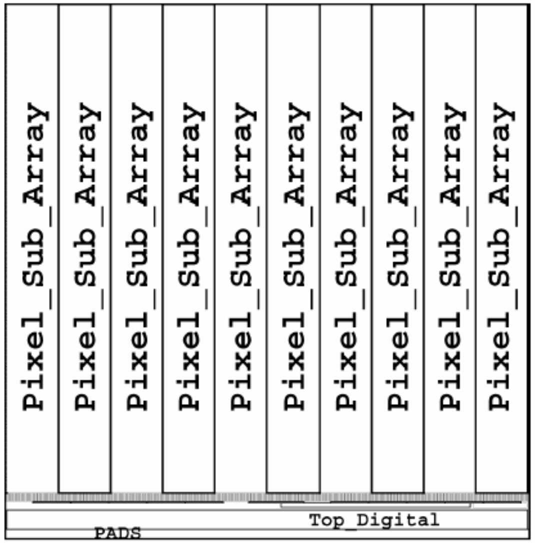


Simplest 2T self-bias pixel
pitch 30 x 30 μm^2

Radiation hard charge collecting diode
(diode with optimized layout)

General view of proposed architecture:

- 10 sub arrays
- Parallel readout
- remote bias and test setting via JTAG
- Fast serial readout
  - up to 100 MHz
  - or ten parallel outputs (@10 MHz)



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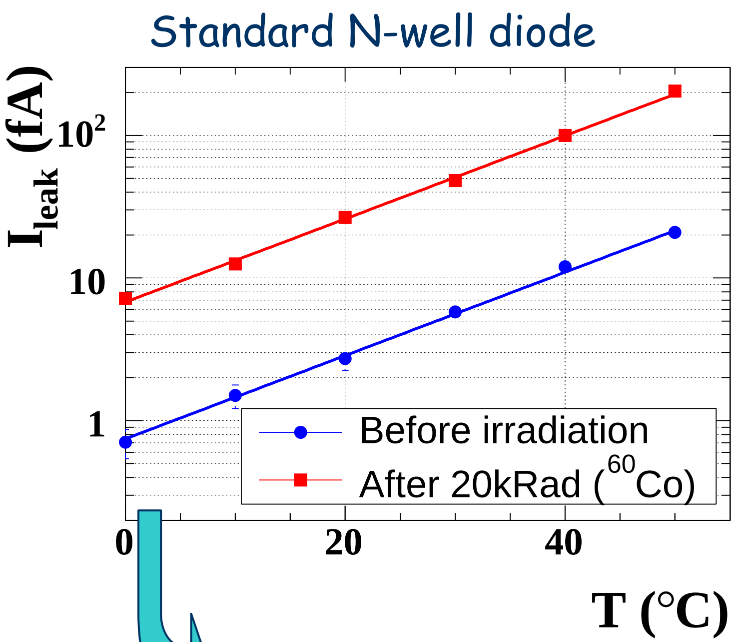

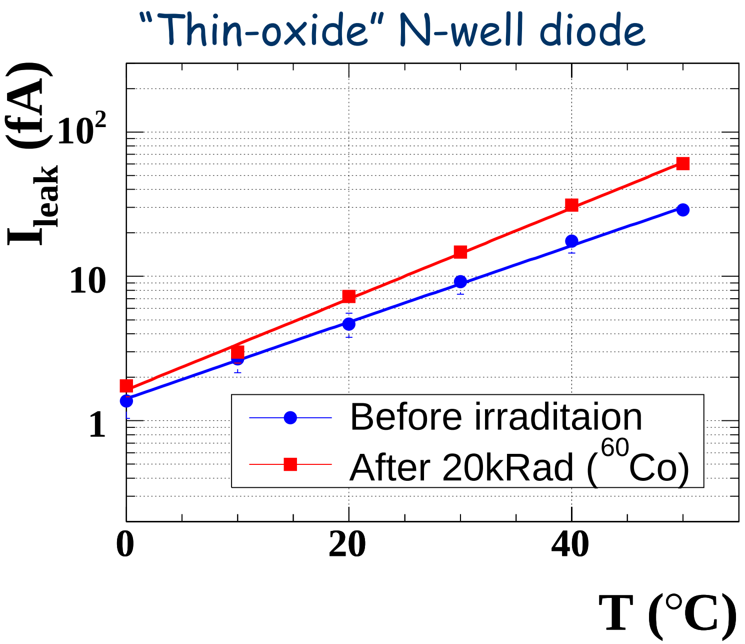

Shot Noise Contribution @ 30°C and @4 ms integration time

ENC_{shot} = 39 e^-

ENC_{shot} = 12 e-

Quite satisfactory level of leakage current increase after irradiation

Self-biased radiation resistive diode layouts are currently being tested (Mimosa XI)
First results very positive
(no noise increase after 20 krad)

Main difficulty

- ✓integration time = 4 ms
- ✓**Room temperature operation: possible**
- ✓Air cooling only
- ✓Ionizing radiation dose in 3years ~20 krad
- ❖Fluence
- ❖Radiation damage in digital part
- ✓Spatial resolution < 10 µm

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MAPS based solutions for ILC

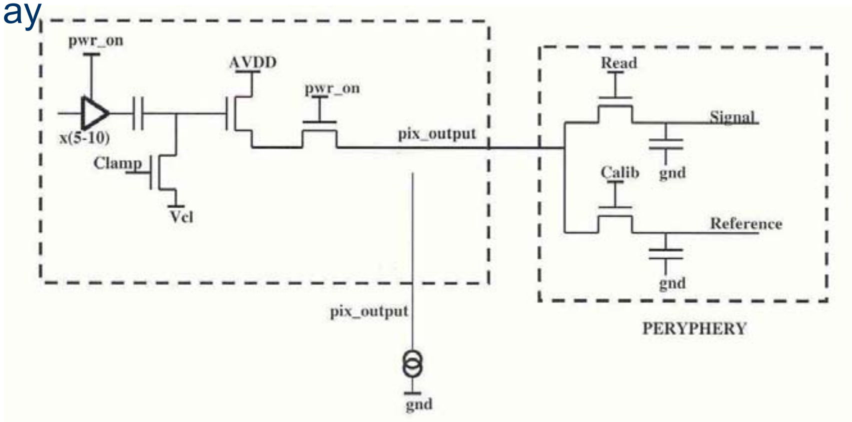
INNER LAYERS

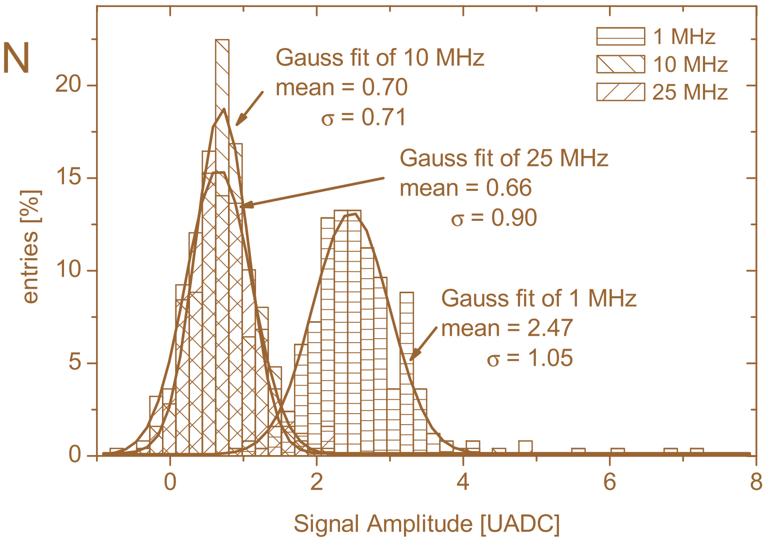
Prototype Mimosa VIII in collaboration with Dapnia/Saclay

- Pixel pitch 25 x 25 μm^2
- Clamping based CDS in pixel
- On-chip FPN suppression
- On-chip discrimination

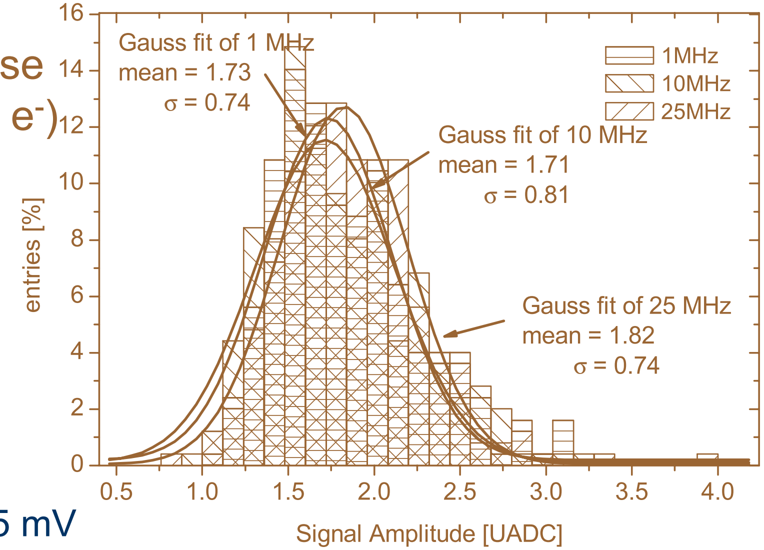
TSMC_0.25

(On-chip discriminators: under tests)





RMS noise (ENC 13 e$^-$)



1ADC = 0.5 mV

First demonstration of feasibility of FPN correction using on-chip real time circuitry
FPN at temporal noise level

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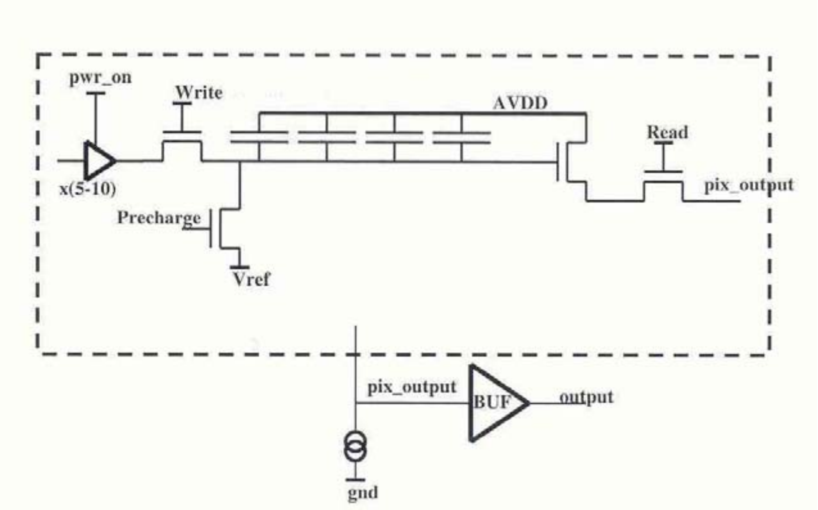
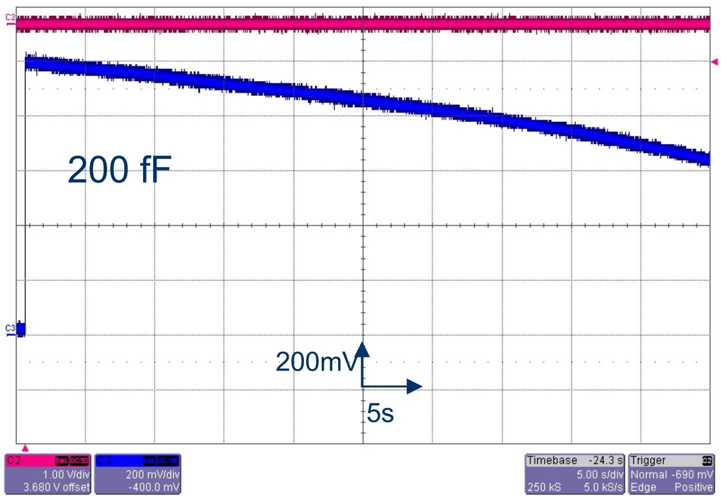
MAPS based solutions for ILC

OUTER LAYERS

Storing several samples in one pixel:
To be extensively studied with next prototype





Discharge time of on-pixel storage capacitors (Mimosa IX)

C (fF)	50 fF	200 fF	400 fF
- 20 % (@ 1 V)	~7 s	~25 s	~50 s

With existing prototype (Mimosa IX):

Pixel with amplifier and two storage capacitors ⇒ measured noise of the readout chain < 10 % of the total noise

Discharge time after irradiation still to be tested

✓Outer layers readout time: 100 – 200 μs
❖ Inner layers readout time: 25 – 50 μs
❖ Dose: < 50 krad/year
✓Spatial resolution < 5 μm ⊕ 10 μm /sin$^{3/2}$θ

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On-pixel amplifiers

- Advantages:
  - Reduction of noise influence from the following readout chain
  - Increasing readout flexibility
  - Increasing on-chip processing power
- Difficulties of amp design in MAPS
  - Basically only one type of transistor can be used in pixel (NMOS)

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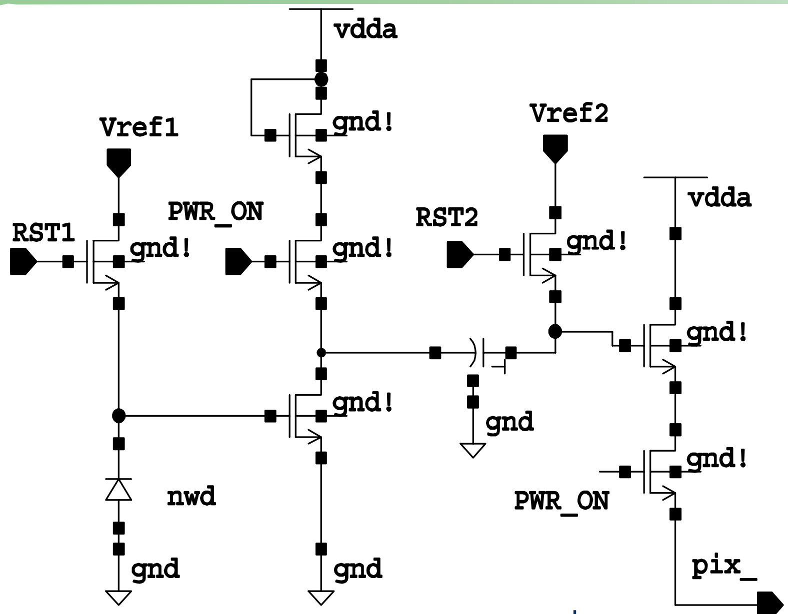
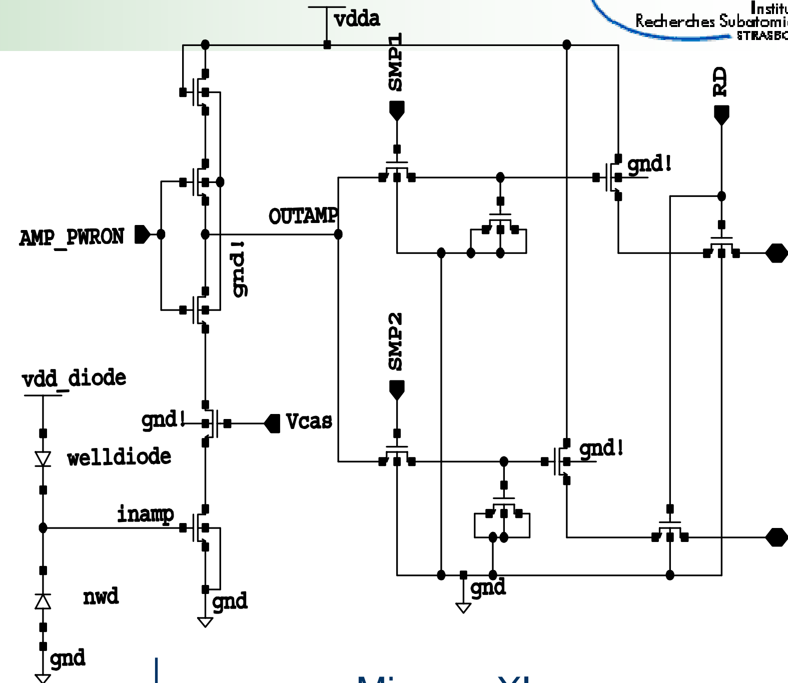
CS and Cascode





prototype	Mimosa VIII (in collaboration with DAPNIA/Saclay)	Mimosa XI
Amp	CS configuration	Cascode configuration
MEMORY	Clamping capacitor	Two memory capacitors
Gain	~14 dB (x5)	~15 dB (x5.5)
Main source of noise (in simulations)	CS ~83%, Load ~12%, switch and SF ~2.5%	CS ~90%, SF ~3%, Load ~4.5%
Measured ENC	(in configurations with the collecting diode of 2.4 x 2.4 μm^2) 18e$^-$	(in configurations with the collecting diode of 4.2 x 4.2 μm^2) 12e$^-$

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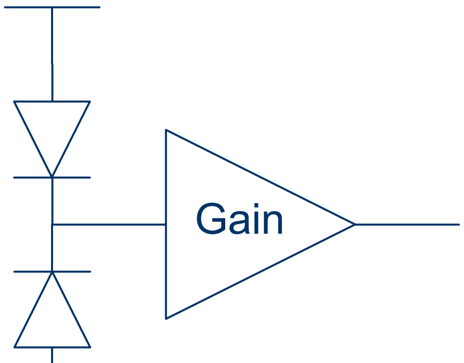
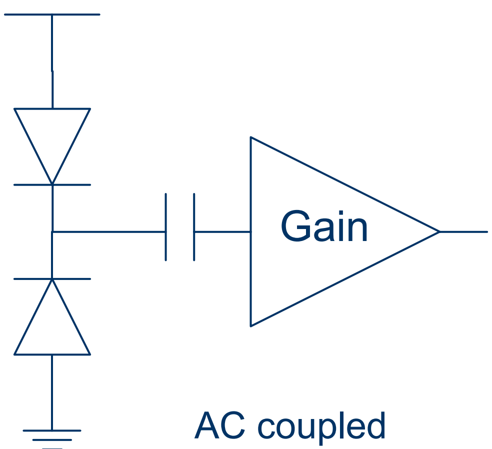
DC coupled and AC coupled on-pixel amplifiers



DC coupled

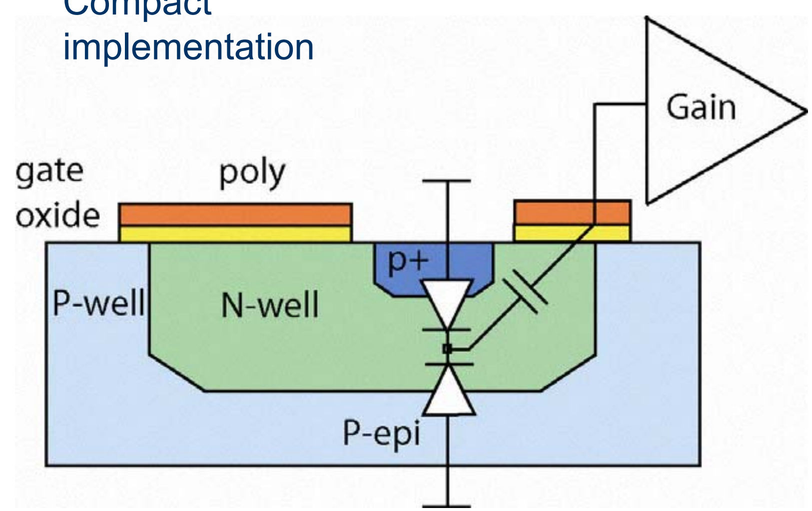
AC coupled amp:

- Separation from power supply of the sensing node
  - Increase of the voltage ⇒ increase of the depleted region ⇒ no influence on the operating point
- Separation from influence of the leakage current
  - Increase of the leakage current after irradiation ⇒ change of the bias on the sensing node ⇒ no influence on the operating point



AC coupled

Compact implementation



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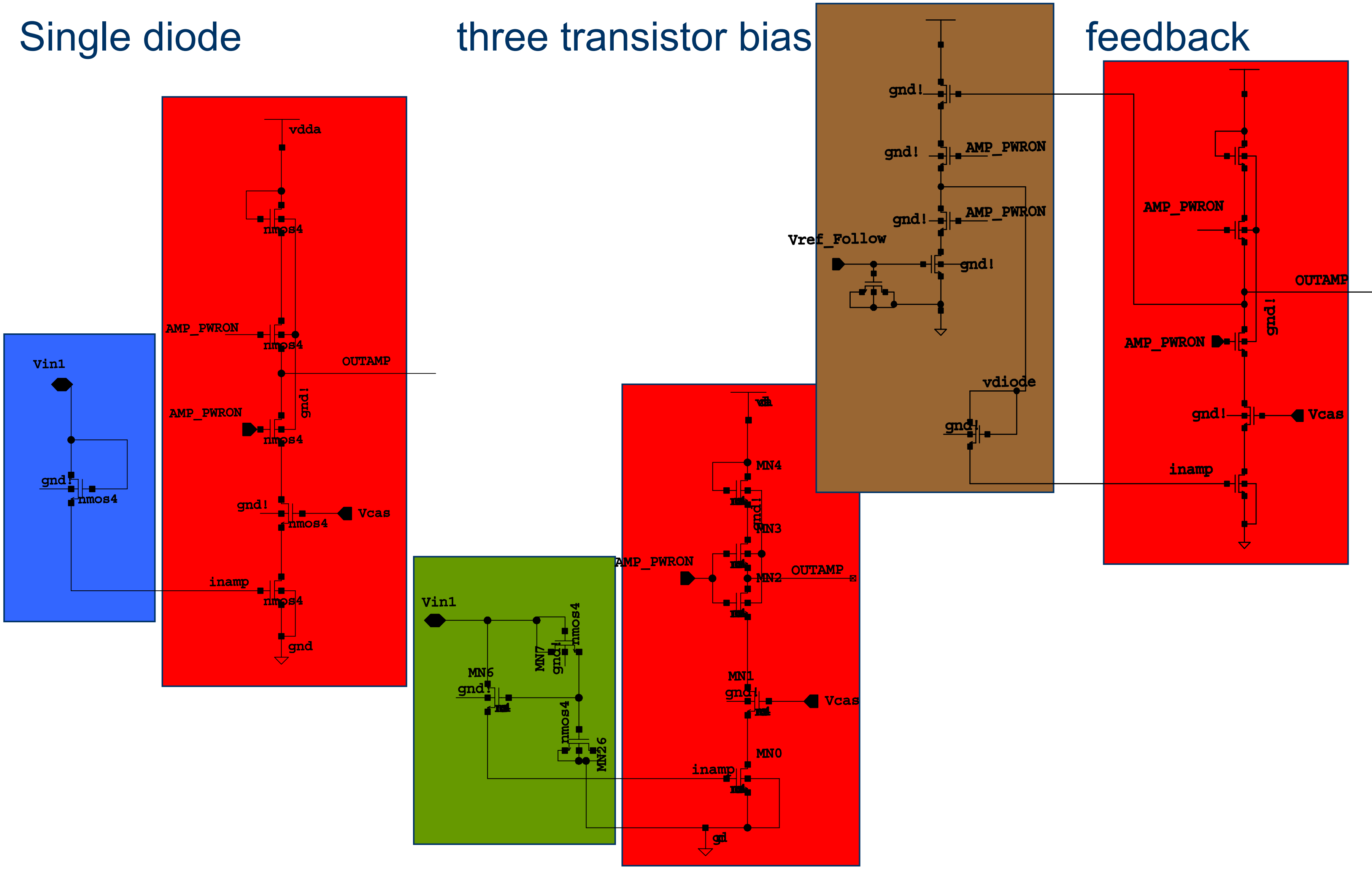
On-pixel amplifiers – AC coupled

- Simple biasing schemes:

Single diode | three transistor bias | feedback



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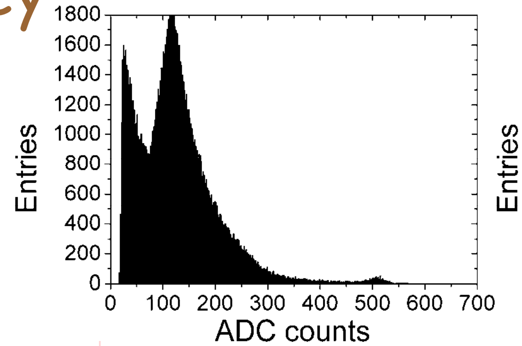
On-pixel amplifiers: DC vs. AC

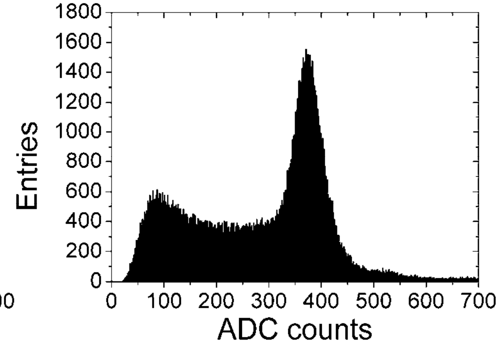
- Charge collection efficiency

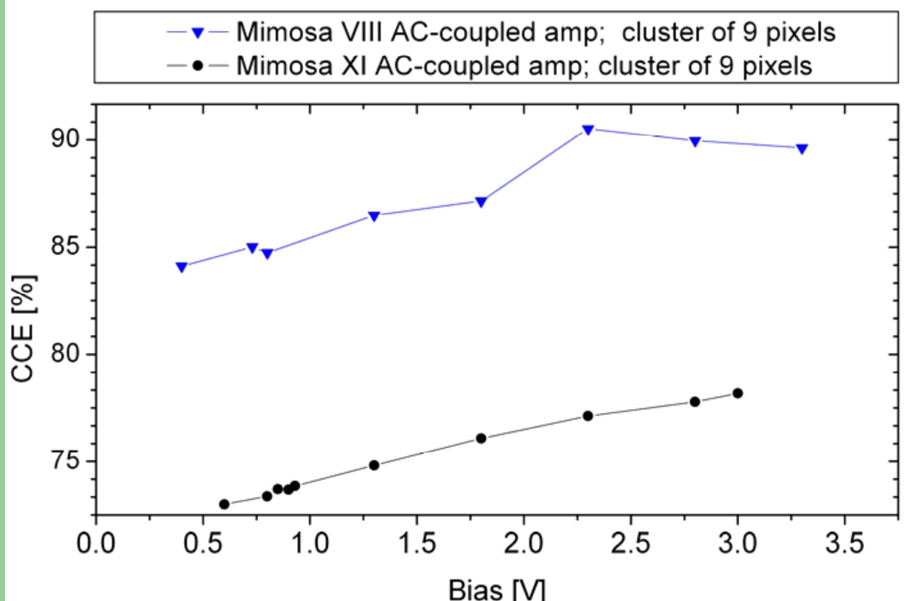
Mimosa VIII TSMC_0.25
Diode: 4.1 x 2.5 μm²
Pixel pitch: 25 x 25 μm²

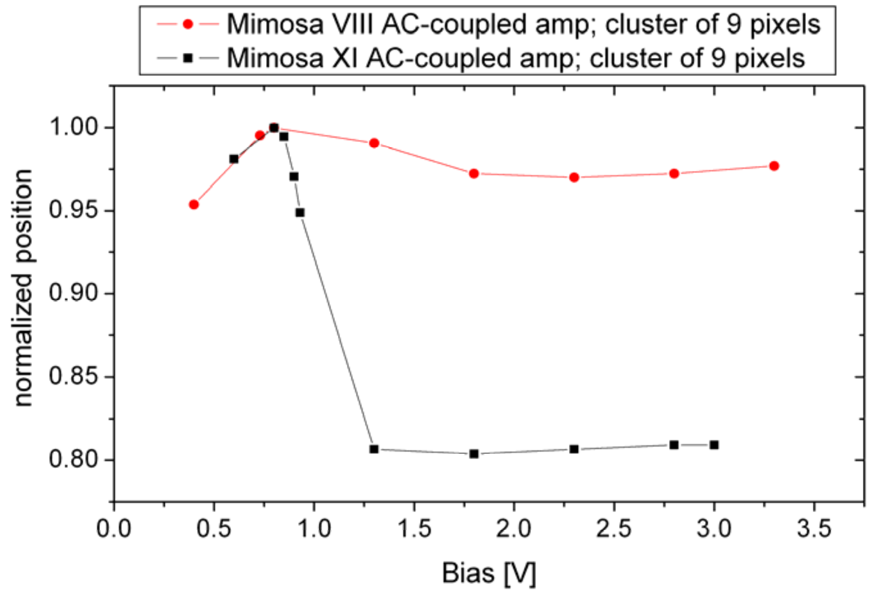
Mimosa XI AMS_0.35
Diode: 4.2 x 4.2 μm²
Pixel pitch: 30 x 30 μm²

➢example









Charge collection efficiency and magnitude of the main peak in 9-pixel clusters in function of bias of charge collecting diode

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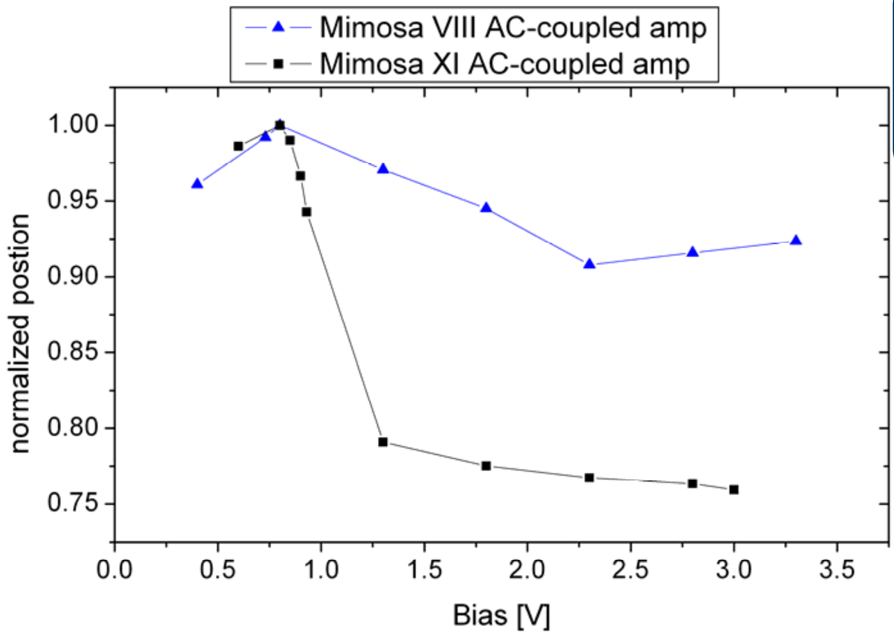
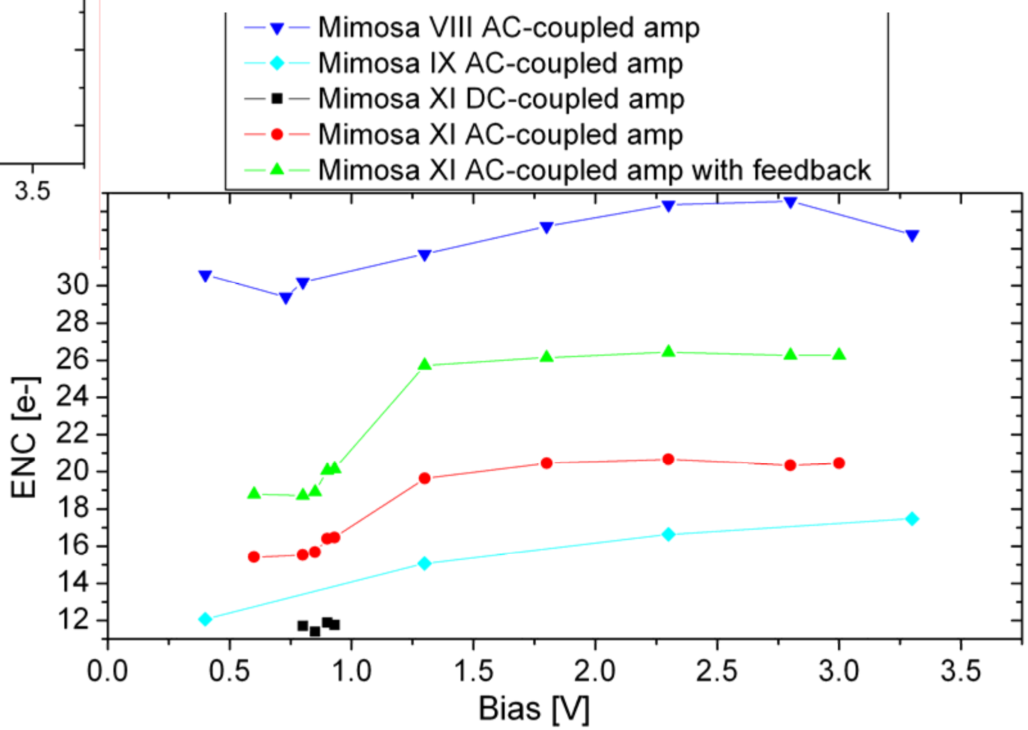
On-pixel amplifiers: DC vs. AC

- Input referred noise

magnitude of the calibration peak and input referred noise in function of bias of charge collecting diode





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Pixel pitch: 30 x 30 μm^2

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SUMMARY

CONCLUSIONS

- MAPS seem to be an attractive solution in many application fields
- VxD @ STAR upgrade is planned to be the first real application in the particle physics domain
- MAPS for SLIM was successfully developed and now is being tested in the complete monitoring system
- On-pixel amplifiers allow increasing readout flexibility and on-chip processing power
- Presented implementation of AC coupling between amplifier and sensing node doesn't improve properties of a sensor as it could be expected $\Rightarrow$ degradation of ENC and S/N ratio

FUTURE PLANS

- Submission of a small-scale prototype for STAR upgrade
- Optimization of MAPS for electron microscopy
- Study of poly – n-well coupling capacitor structure for better understanding of its properties
- MAPS for ILC: see "A Vertex Detector for the ILC based on CMOS Sensors" by A.Besson @ Vertex Detectors