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# CMOS Monolithic Active Pixel Sensors for high resolution particle tracking and ionizing radiation imaging

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***LEPSI and IReS, Strasbourg, France***

***SUCIMA:** Silicon Ultra Fast Cameras for Electron and Gamma Sources in Medical Applications,*

*E.C. Contract N. G1RD-CT-2001-00561 (France, Germany, Italy, Switzerland, Poland)*

## Outlook

- **Principle of CMOS MAPS**
- **Short reminder of measured tracking performance**
- **Readout strategy for future tracking application**
- **Radiation imaging using MAPS**
- **Conclusions**

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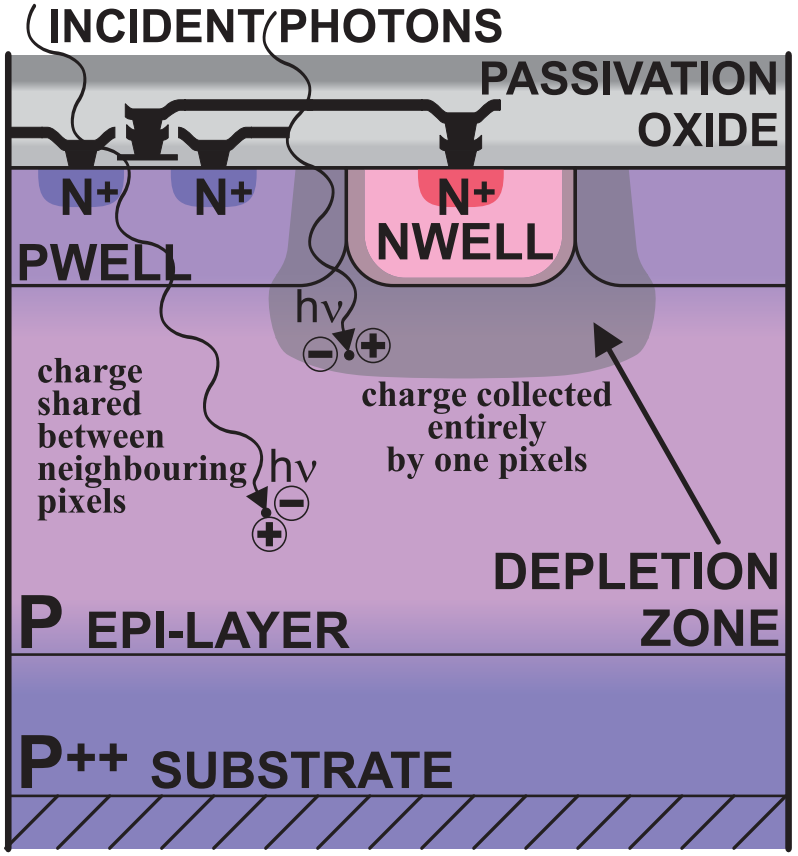
# CMOS Monolithic Active Pixel Sensors (MAPS) principle

"From digital cameras to particle tracking device"




**-The active volume (epi-layer, ~10 µm thick) is underneath the readout electronics, providing 100% fill factor**

**-The charge generated by ionization is collected by the n-well/p-epi diode**

**-Charge collection is achieved by the thermal diffusion**

**The device can be fabricated using a standard, cost effective and easily available twin-tub CMOS process on epi substrate. No post-processing (e.g. bump-bonding)!**

**System-on a chip approach possible**

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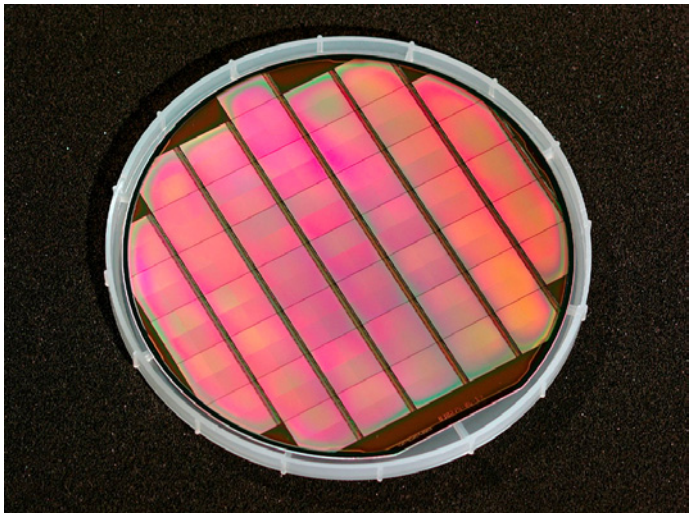
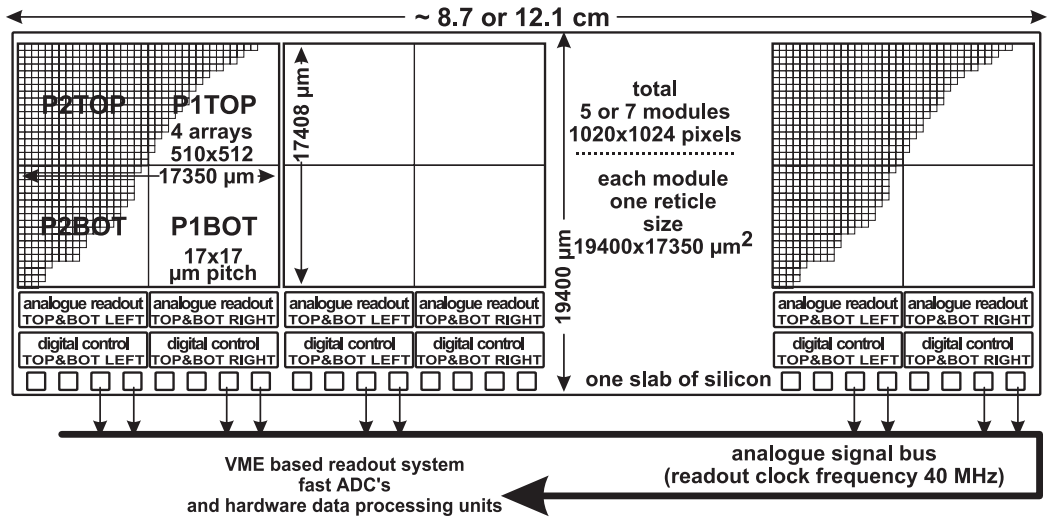
# Wafer scale MAPS prototype: Mimosa5






**Maximum allowed size of a circuit in a standard CMOS process: ~20x20 mm$^2$ (reticle)**

**Reticle stitching is needed, in order to get a larger device (a ladder, 10x2 cm$^2$)**

**MIMOSA5**

**Each reticle is an independent circuit. Periphery logic and bonding pads layout along one side. Simplified stitching of up to 7 reticles in one direction. Still some problems with a yield (~20-30%) but it can be solved (according to digital light imager manufacturers).**

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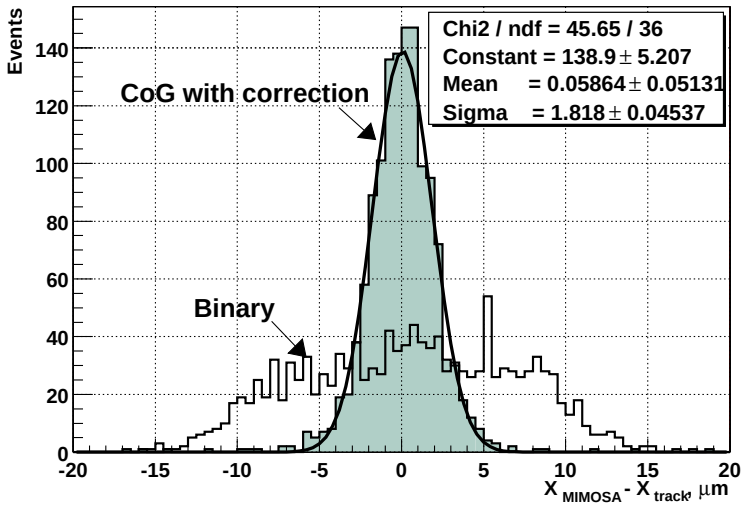
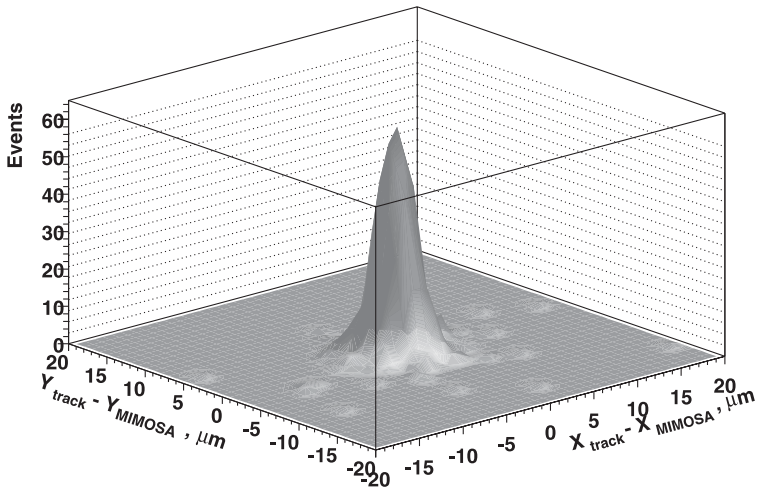
# CMOS MAPS particle tracking performance (20 µm pitch)




**ENC ~10 electrons: S/N>30**
**Efficiency (5σ seed cut): $\varepsilon_{MIP}$ > 99 %**
**Spatial resolution: σ = 1.4 µm**

**Demonstrated on several devices in various submicron CMOS processes:**

**AMS 0.6 µm, 14 µm epi**
**Alcatel 0.35 µm, 4 µm api**
**AMS 0.35 µm, no(!) epi**
**…**
**TSMC 0.25 µm, 8 µm epi**
**(LBL team)**

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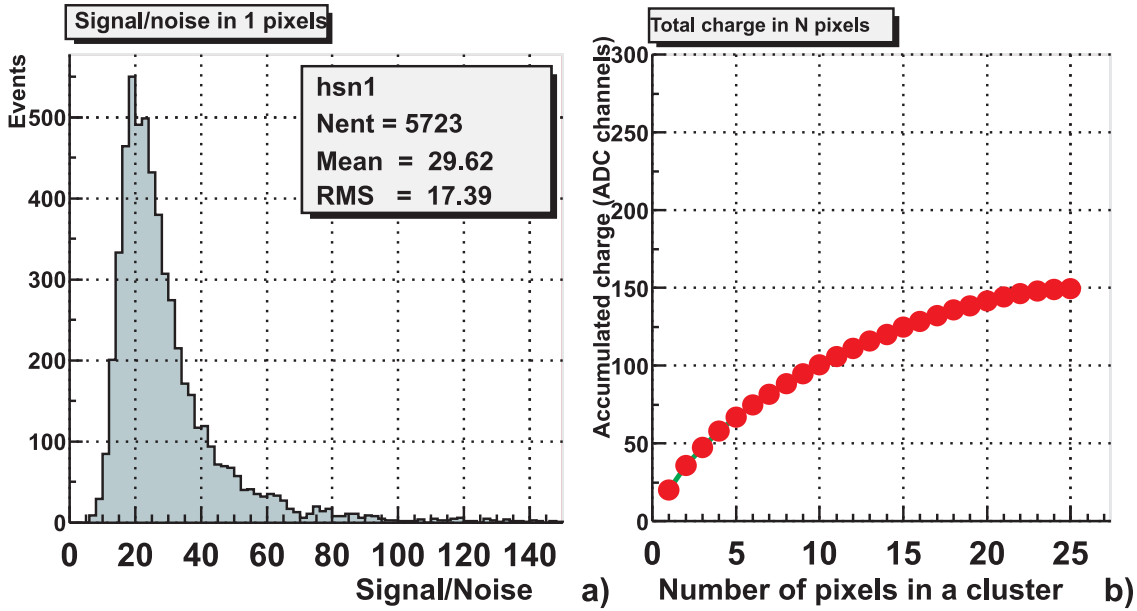
# MIMOSA-4 (no-epi substrate) test results:

**0.35 mm AMS process without epitaxial layer**
**but with low doping (high resistivity) substrate**




**Observed performances with 120 GeV/c p- at CERN-SPS:**

- Detection efficiency ~99.7%
- S/N ~30 but charge is wider spread
- Spatial resolution ~4 μm (20 μm pitch)

**Technology without epitaxial layer (future?) seems worth investigating and optimizing**

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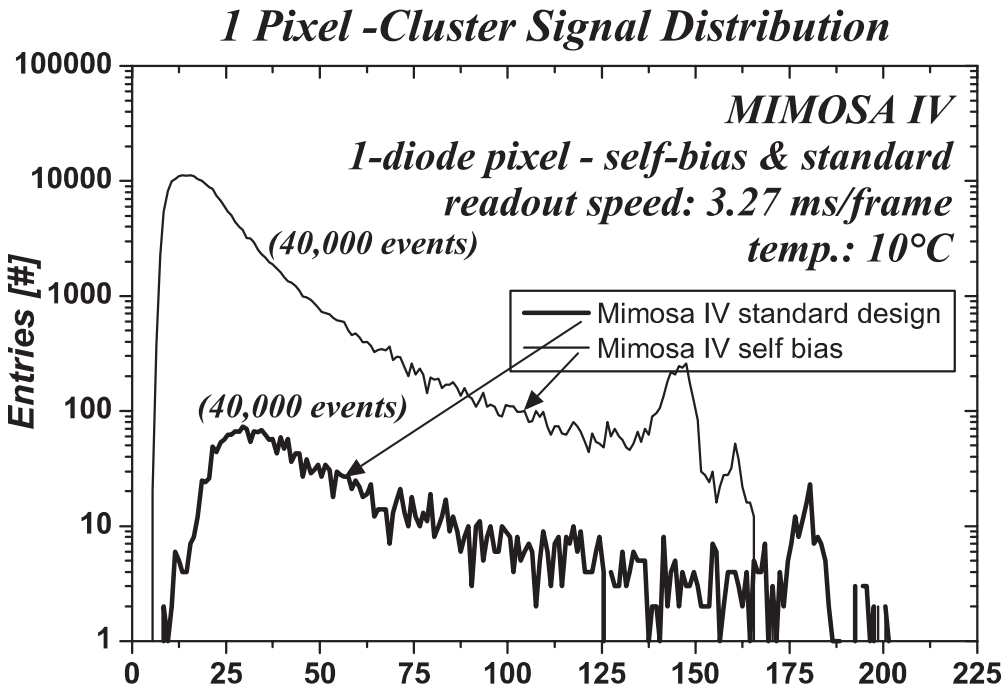
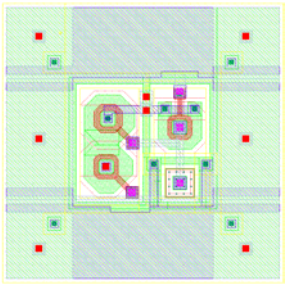
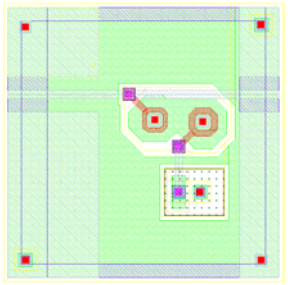
# Be prepared for surprises with some CMOS processes…
## Mimosa4 case



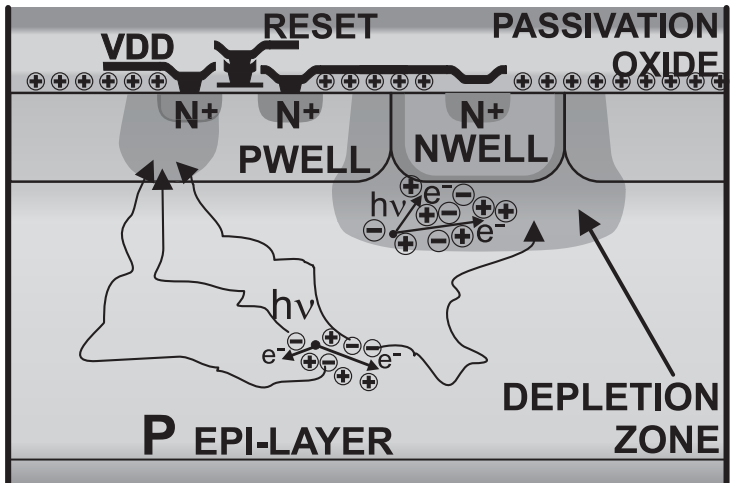

**Strong layout dependence!**



**Standard 3-T**



**Self-biased 2-T**




**Hint to explain post irradiation performance?**

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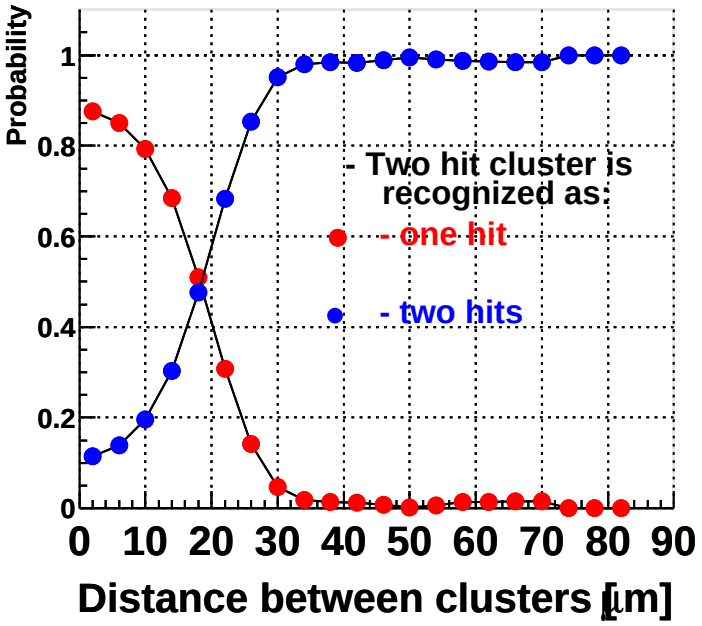
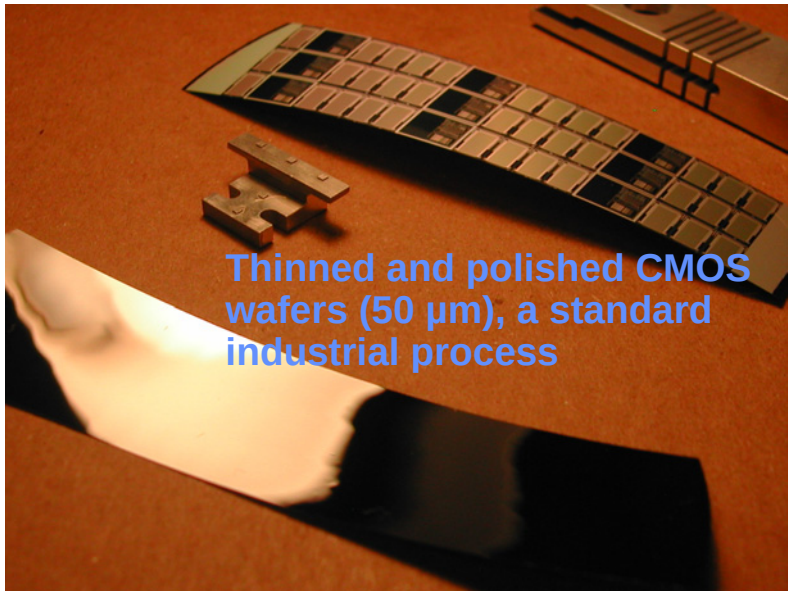
# Keeping high tracking performance to low momentum particles




**Two-track resolution: 30 μm (simulation on real data)**

1. **Thinning the substrate to 50 μm (or less)**
2. **Low mass (air?) cooling: keeping down the power dissipation (~100 mW/cm$^2$)**



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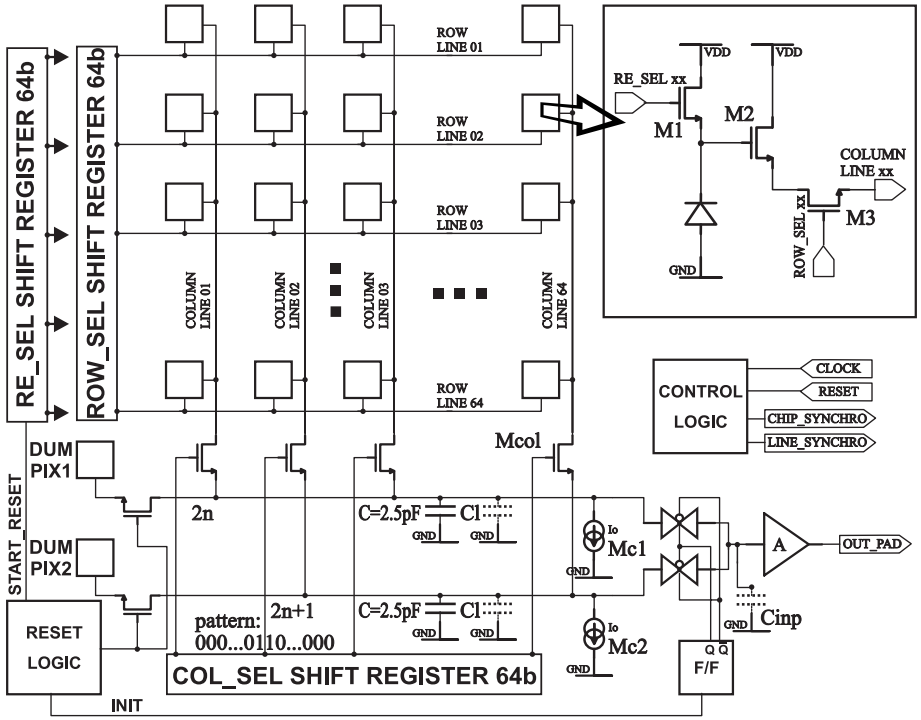
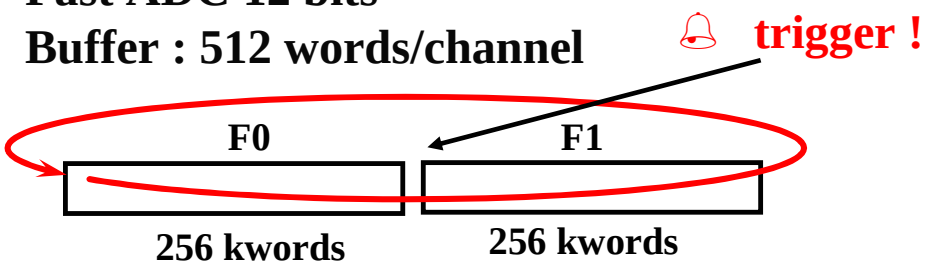
# The simplest readout electronics: diode + 3 transistors/pixel




1. Reset in order to inverse bias
2. Continuous serial addressing and readout (digitisation) of all pixels
3. Keeping two successive frames in external circular buffer
4. Following reset when needed (removing integrated dark current)
5. After trigger (or in a real time)), simple data processing in order to recognise hits

**Fast ADC 12 bits**

**Buffer : 512 words/channel**



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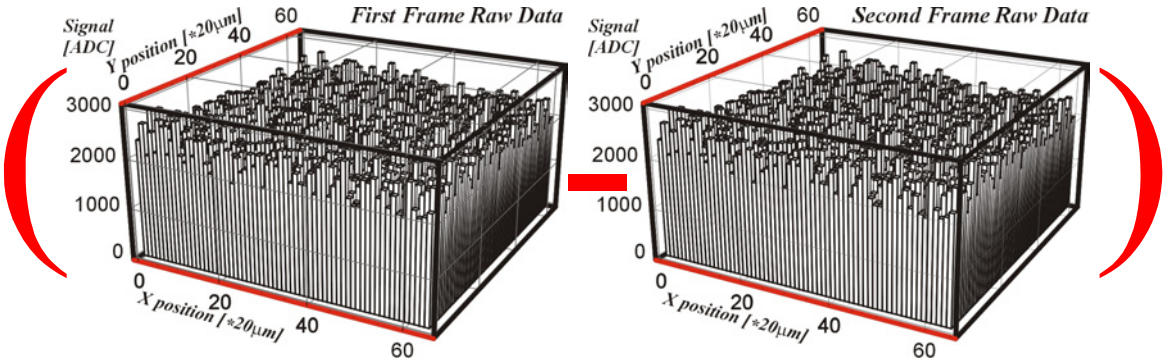
# Data processing: (Digital) Correlated Double Sampling



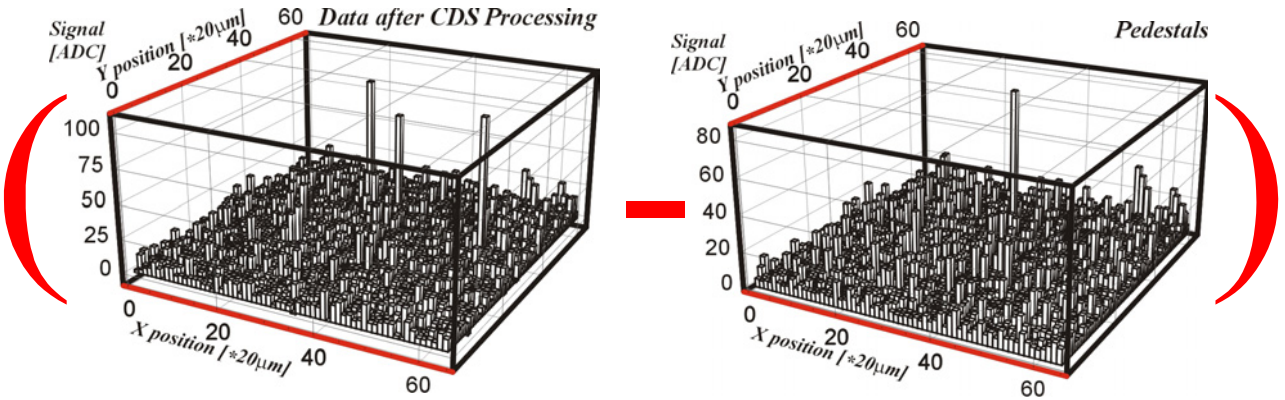

fram e 1) fram e2)

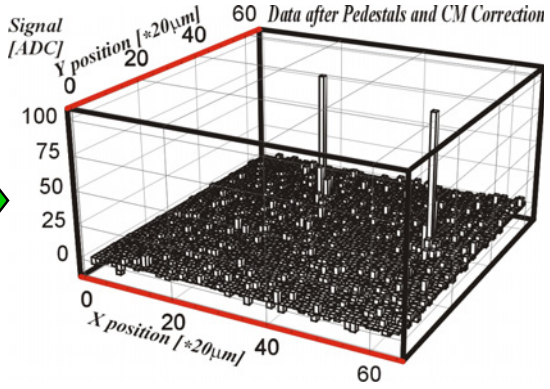
**(frame2 - frame1) subtraction**

**Useful signal on top of Fixed Pattern DC level**

**Fixed Pattern dispersion: ~100 mV**

**Typical signal amplitude: ~1mV**




fram e2 – fram e1) **Pedestal (dark current) subtraction**

**Hit candidates!**

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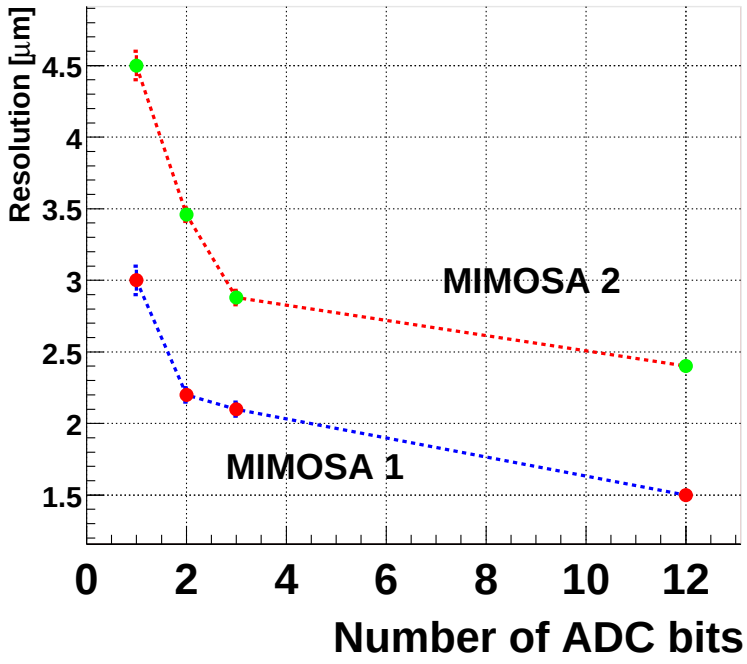
# External CDS data processing for a typical pitch of 20 µm (250 kpixels/cm$^2$)




1. **Efficient cancellation of fixed pattern (DC level dispersion between pixels)**
2. **kTC (reset) noise totally removed (kTC is a dominating noise source)**
3. **Low power dissipation, dominated by an analog output buffer (~50mW)**

1. **Slow! ("5 ms/cm$^2$ & 50 MHz")**
2. **High precision (>10 bits) digitisation required, NOT really needed for tracking precision (see left)**
3. **A lot of external, reference memory**

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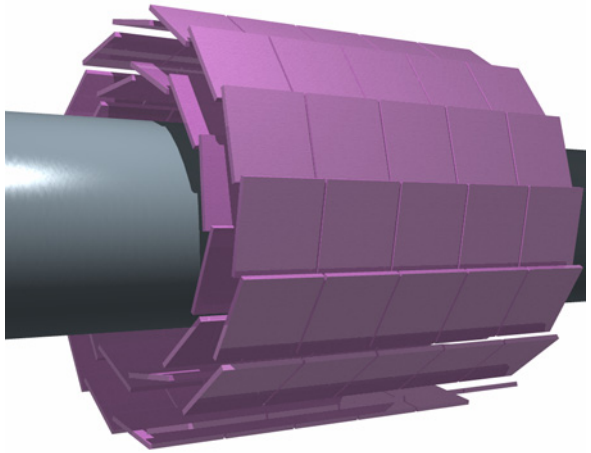
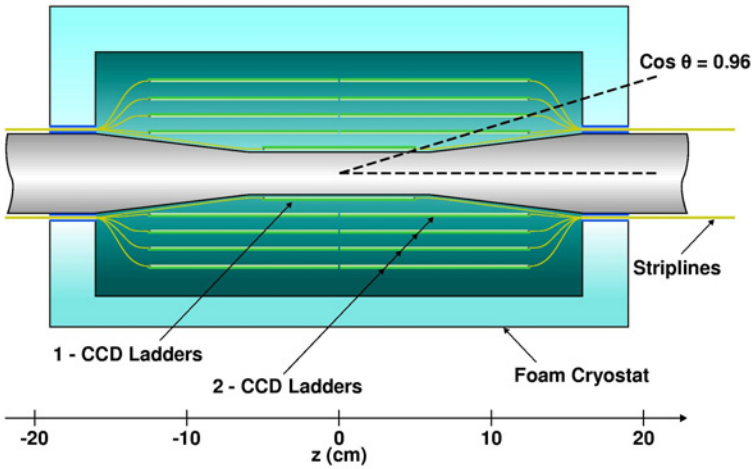
# Future experiments requirements



## STAR μvertex detector

1. First upgrade (x4 present luminosity, 2006):
   10 – 20 ms readout (integration) time
2. Second upgrade (x40 present luminosity, 2008):
   2 – 5 ms readout (integration) time




## TESLA Vertex Detector*

1. Outer layers readout time: 100 -200 μs
2. Innermost layer readout time: 25 -50 μs

*NLC/JLC: t~10 ms

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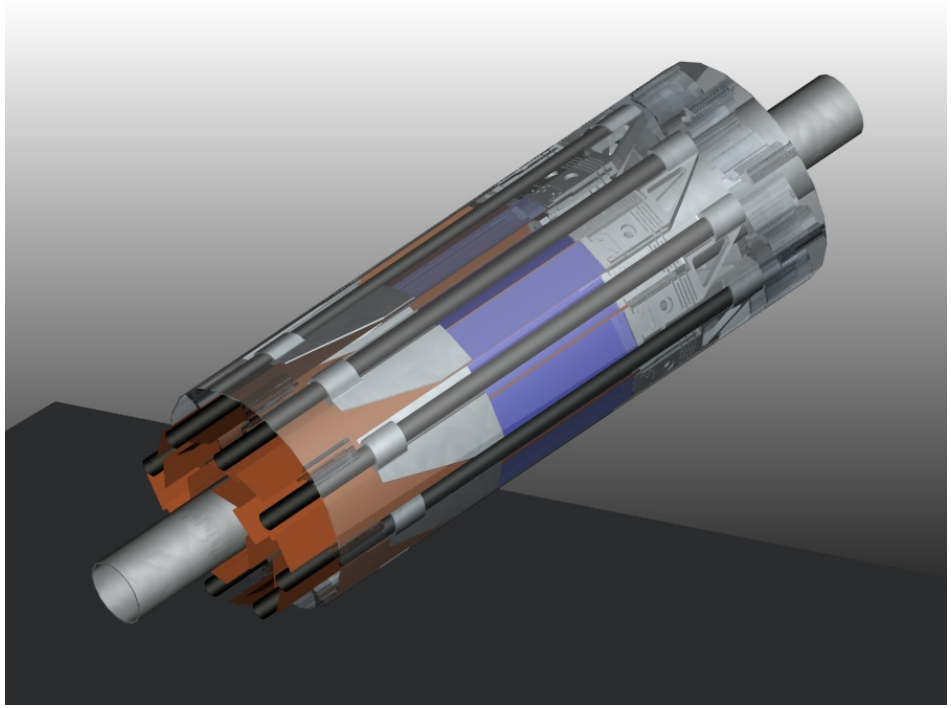
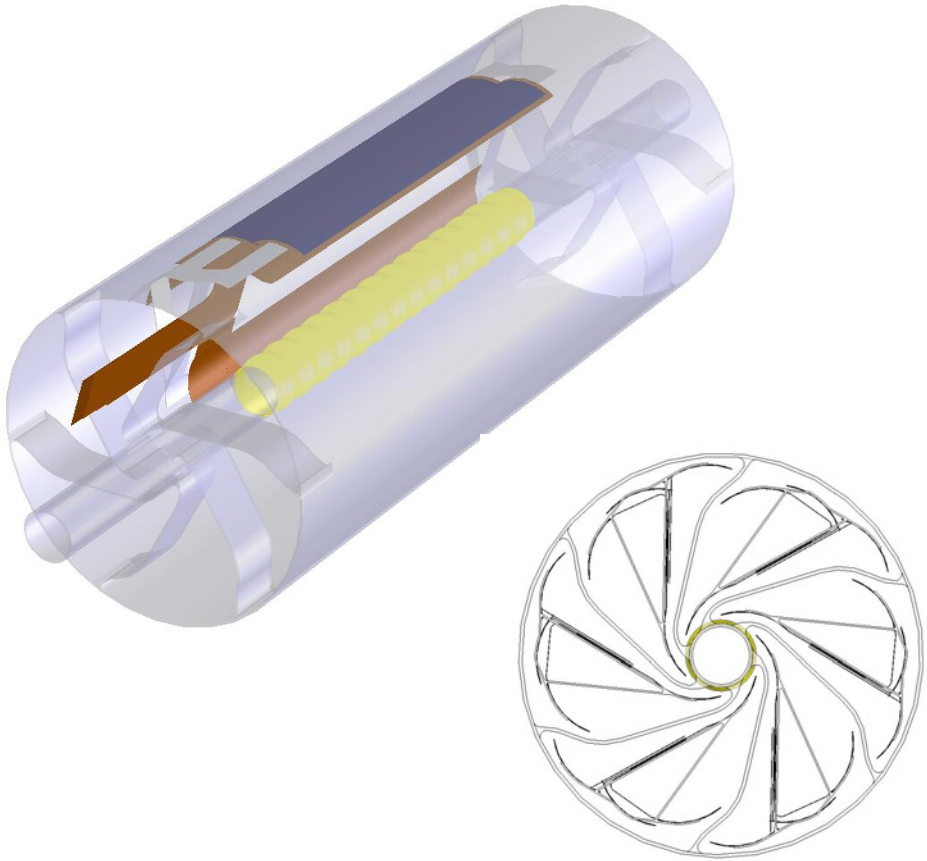
# Mechanical concepts of STAR Micro vertex upgrade using ultra-thin CMOS MAPS *



Tension concept



Self supporting Venetian blade concept

* Curtsey to Howard Wieman, LBL, STAR group

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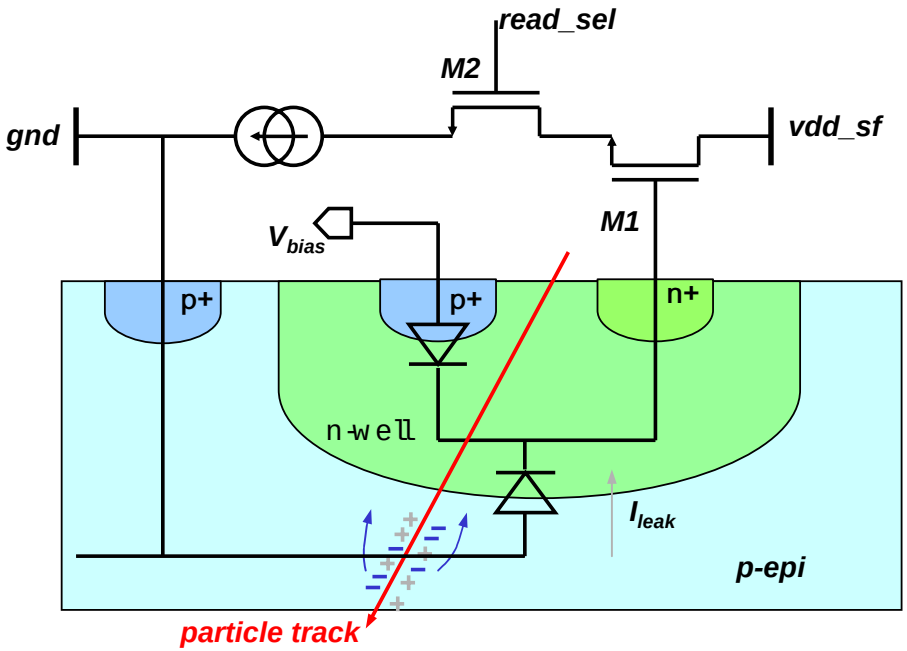
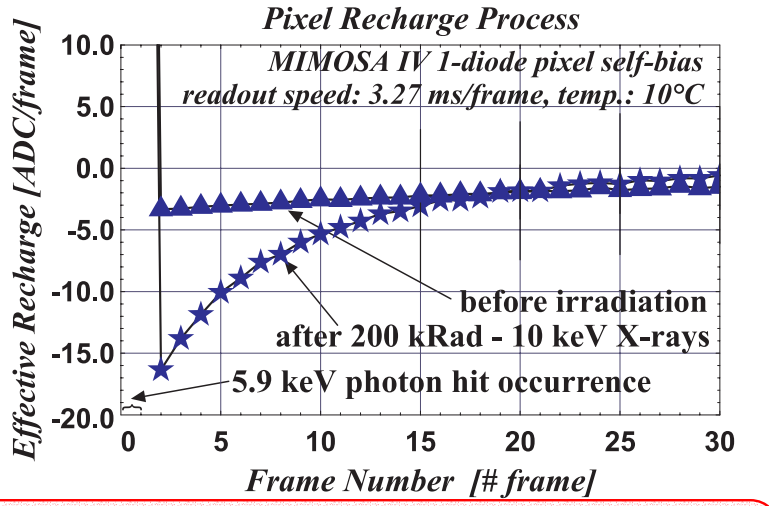
# Modified sensing elements: self-biasing diode




## DC level stabilization

**RESET transistor replaced by a forward-biased diode, equivalent of a ~TeraOhm resistor for a ~fA (typical) leakage current**




## Typical RC constant: tens of ms (even after irradiation)

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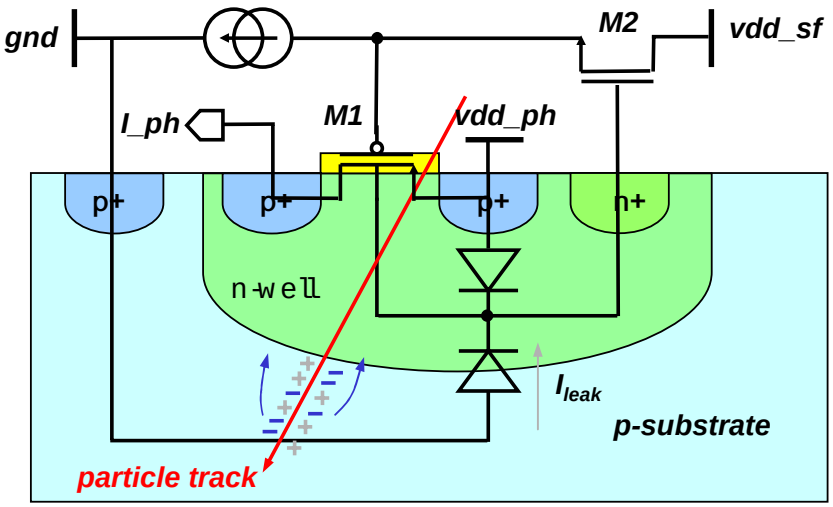
# New charge sensing elements: PhotoFET




**Charge collected at the N-well affect the threshold voltage of a pMOS transistor and modulates its current: signal amplification**

**-Charge-to current amplification**

**-High transconductance = high sensitivity**

**-Low noise/large collection area**

## First prototype test results

**Sensitivity: 330 pA/electron**

**ENC: ~5 electrons**

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# Possible direction to increase MAPS readout speed

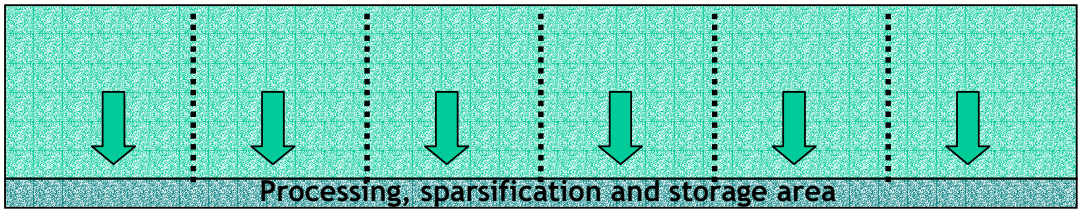
## Full parallel processing: all pixels always active (dissipating power)

1. Power dissipation too high! A few µA/pixels gives ~10 µW/pixel*, i.e. > 2 W/cm$^2$!
2. Limited choice of architecture: NO PMOS transistors allowed (except periphery)
3. Limited surface (for a "standard" 20 µm pitch)

* Our estimation of a lower limit for any realistic (today!) processing circuit

## Column parallel processing: only one row a time active

1. Power dissipation reasonably low, usually dominated by a processing circuit at the bottom of each column, where both transistor types are allowed
2. Modest processing effective speed (~10 MHz) provides already an interesting speed gain (frame readout in 100 µs, for a column of 1000 pixels)



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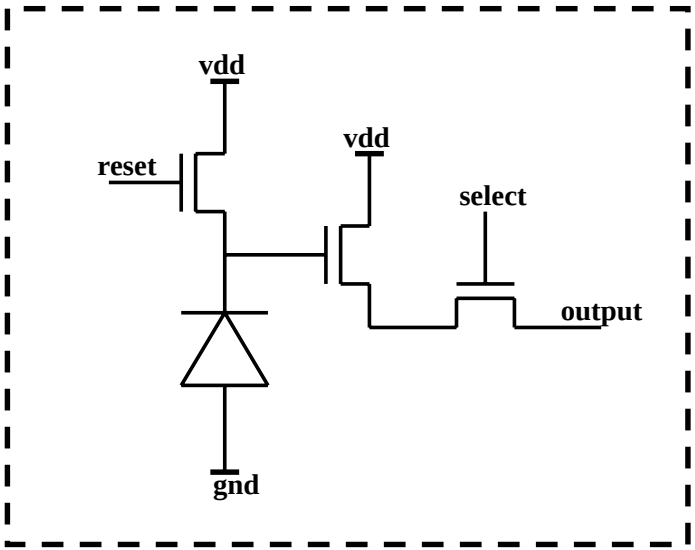
# Possible column parallel processing implementation

**Three essential processing steps needed**

1. **Fixed pattern removal (equalisation of a DC output level for each individual pixel)**
2. **Signal discrimination or low precision (2-3 bits) digitisation (at the end of each column)**
3. **Data storage/transmission**




**1. Readout-Reset-Readout**

**Rather hopeless for tracker, because of dominating kTC noise* and resetting precision**

*** kTC noise on 15 fF: 34 electrons**

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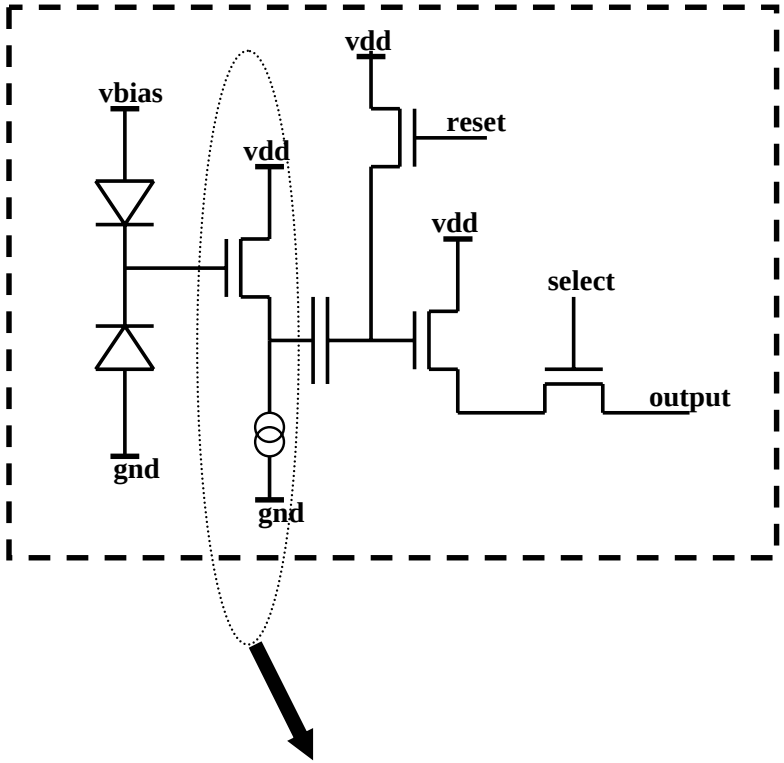
# Possible column parallel processing implementation (pixel architecture)




To be replaced by an amplifier x5?

## 2. Readout-Clamping-Readout CDS

**Rather fast (~10 MHz effective), still simple architecture, promising if signal amplified (x5)?**

**Simulation, prototype soon (collaboration DAPNIA/IReS-LEPSI)**

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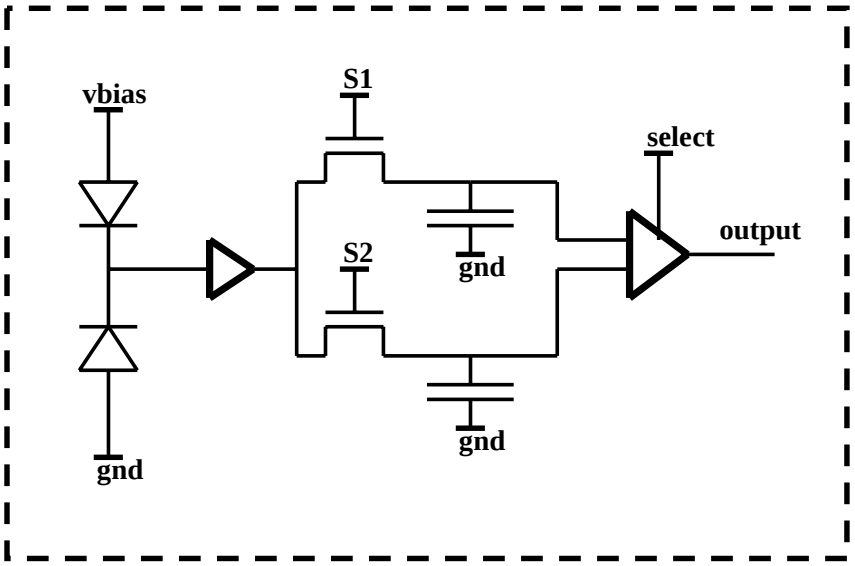
# Possible column parallel processing implementation (pixel architecture)




## 3. Analog on-pixel CDS

**Starts to be complicated.**
**All details count (charge injection, threshold dispersion, biasing…)**

**Easier with PhotoFET and current memory?**

**First (voltage memory) prototype in testing, second (PhotoFET and current memory) close to submission**

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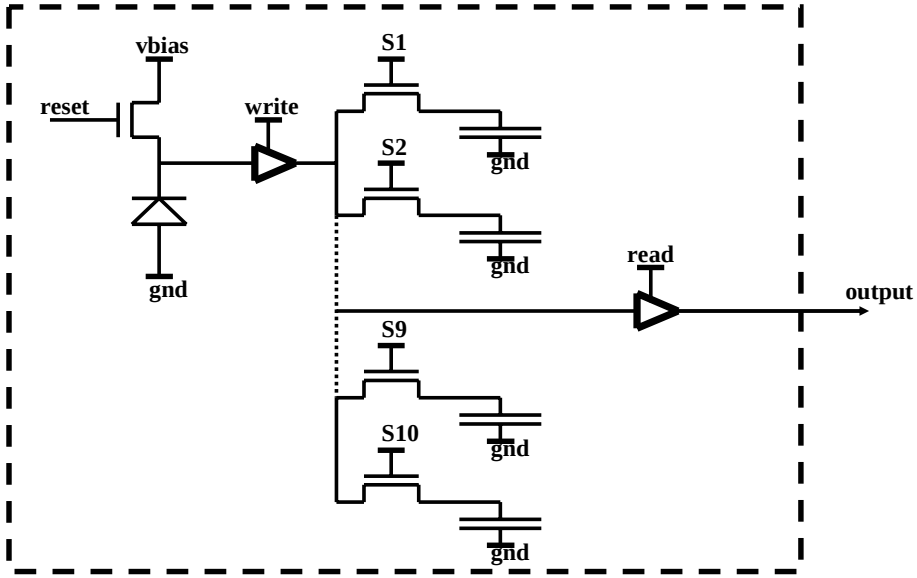
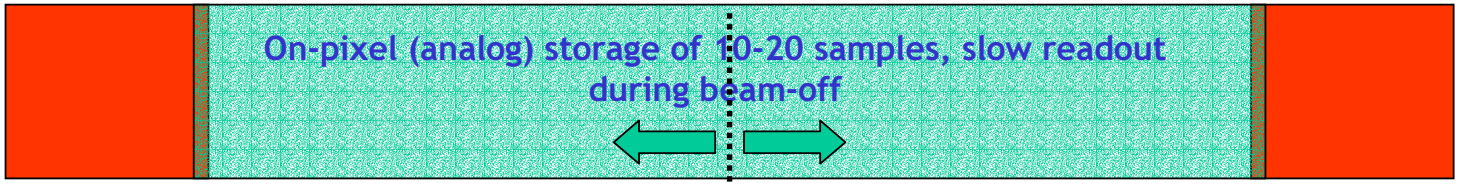
# Possible column parallel processing implementation (pixel architecture)

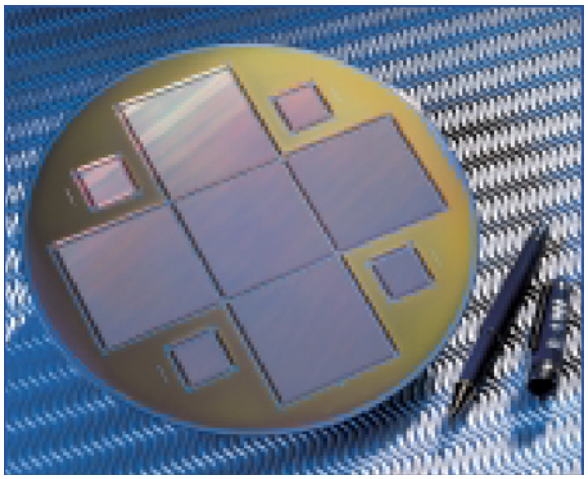



## 4. Multi-frame on-pixel buffering

**To be demonstrated, limit on the number of frames (10?) implementation may be easier with PhotoFET and current memory cells**

## RAL prototype (FAPS) Status???



**Real stitching is mandatory in this case, but such a technology exists in CMOS imagers industry!**

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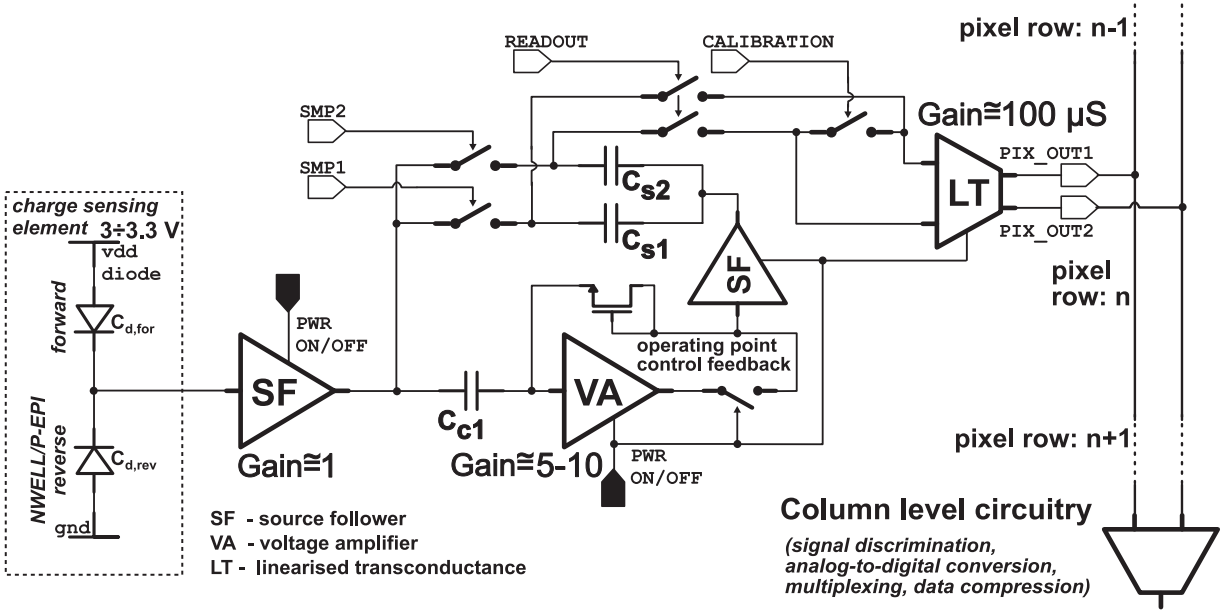
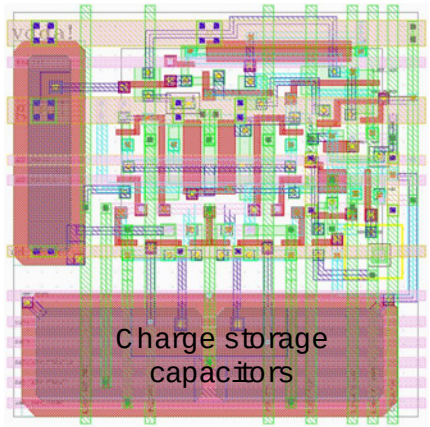
# MIMOSA-6: first sensor with integrated functionality
# IReS-LEPSI/DAPNIA collaboration




**Amplification (x5.5), AC coupling, analog memory (2 cells), on-pixel CDS, current output buffer, discriminator per column**

**128 pixels/column, 5MHz effective readout frequency, Power dissipation ~500 µW/column**




**Pixel layout:**
**28x28 µm$^2$**
**29 transistors**

**First results:**

**ENC = 15 electrons**
**Comparator offset (input referred) < 1mV**
**Pixel-to-pixel output voltage dispersion too high!**

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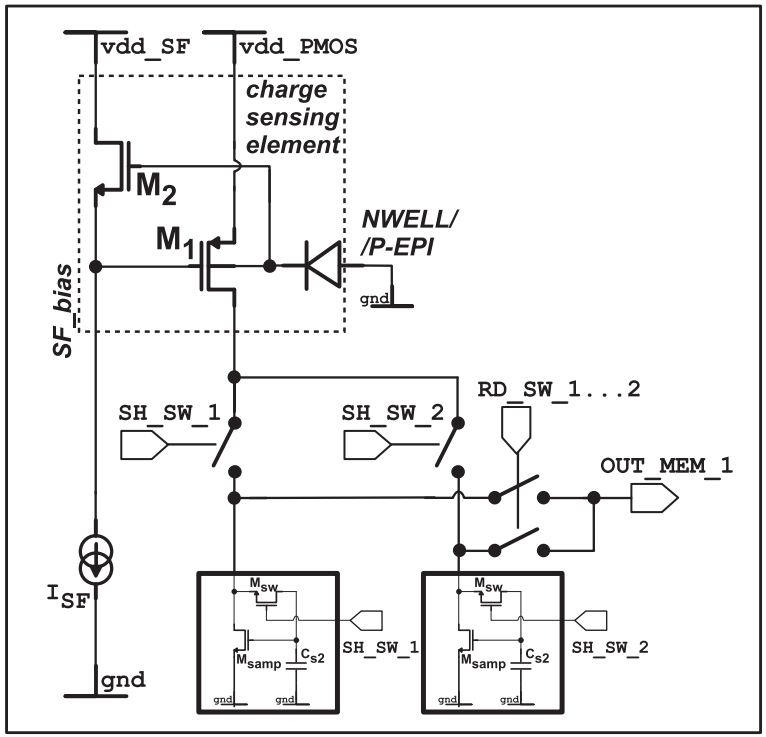
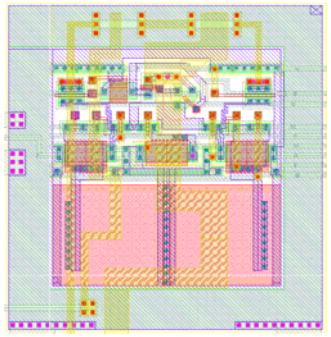
# MIMOSA-7 (submission in June): PhotoFET based sensor




Amplification, analog current memory (2 cells), current output of each stored value,
Per column: transresistance difference amplifier (CDS function) and 3 bits Wilkinson ADC

128 pixels/column, 3 MHz effective readout frequency, power dissipation ~700 µW/column



Pixel layout:
26x26 µm$^2$
15 transistors

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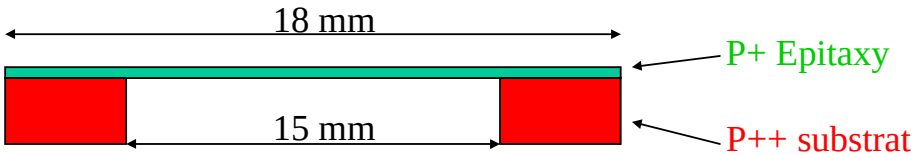
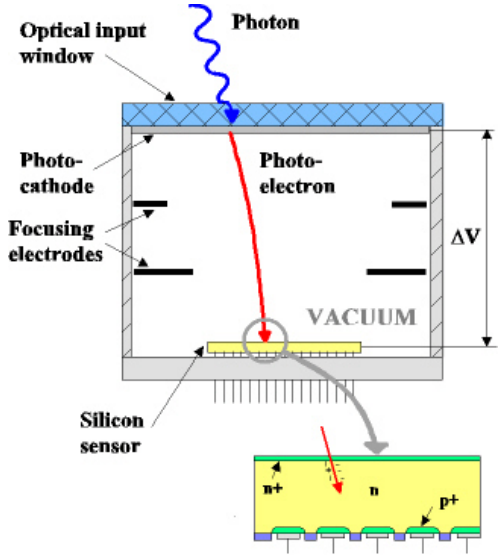
# Monolithic CMOS Pixel Detectors for Radiation Imaging? A lot still to be done!

1. Visible light: first and the most important commercial application!
2. X and γ imaging: not very appropriate (except dental imagers using scintillating converter)
3. α and electron (β) imaging dosimetry : see SUCIMA Collaboration contribution
4. Neutron imaging (using Be or Ga converter foils)




**Back - thinning for low energy electrons imaging**




**Hybrid Photo Diode (HPD) ---> single photon imaging**

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# Conclusions

☑ Excellent tracking performance of CMOS pixels successfully demonstrated with small and large scale prototypes: ε~99%, S/N~20-40, σ~1.4-2.5 µm @ 20x20 µm$^2$ pitch

☑ Easy access to processes with epitaxial layer (e.g. TSMC 0.25 µm with 8 µm thick epitaxial layer)

☑ Cost effective solution for a complicated, already well performing and promising device (~2-3 k$/ 8'' wafer ⇨ 10-15 $/cm$^2$)

☑ directions to investigate:

- readout speed improvement, data processing (sparsification) on-a-chip OR data buffering before slow readout
- optimization of the sensitive element - alternative charge sensing structures
- yield optimization of a large size chip, thinning to 20-50 µm, on-wafer stitching, mechanical mounting and cooling
- radiation hardness understanding/improvement (already OK for STAR and TESLA)

☑Intensive R&D program at Strasbourg on CMOS MAPS for STAR and TESLA VD, in collaboration with several other centers (Rome, DESY, CERN, BNL, LBL…)

☑R&D program for radiation imaging application (SUCIMA, Euromedim…)