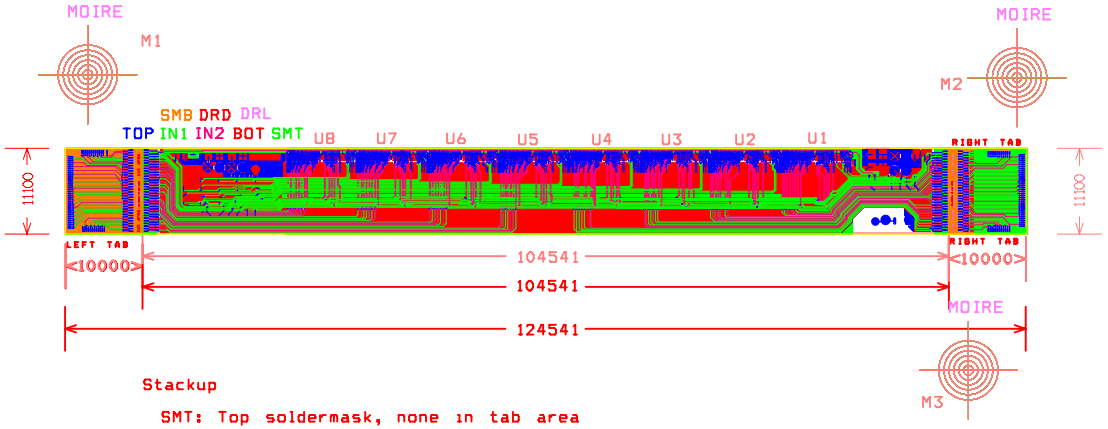


Stackup

SMT: Top soldermask, none in tab area
TOP: Top Metal Layer, top traces and GND plane
IN1: metal layer 2, broadside coupled differential traces & edge couple differential traces
IN2: metal layer 3, broadside coupled differential traces
BOT: bottom metal layer, Power Plane
SMB: Bottom soldermask, none in tab area

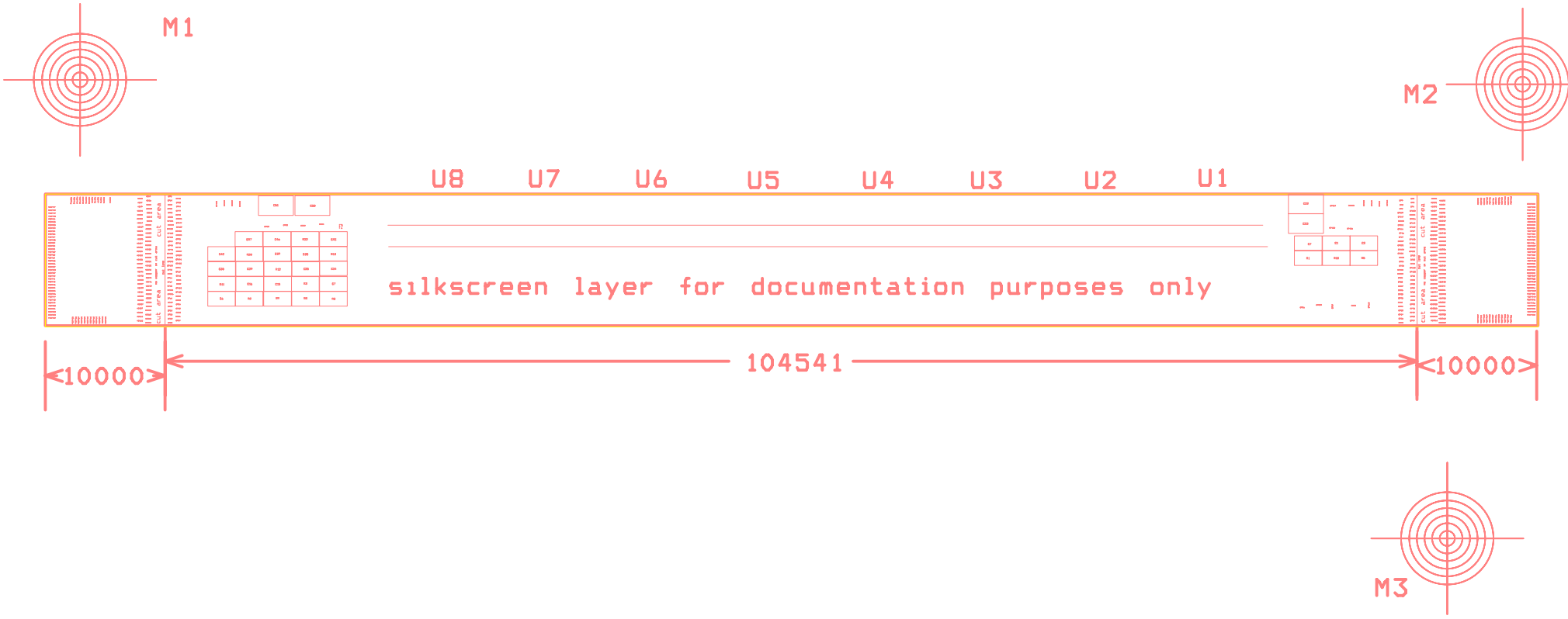
silkscreen layer for documentation purposes only

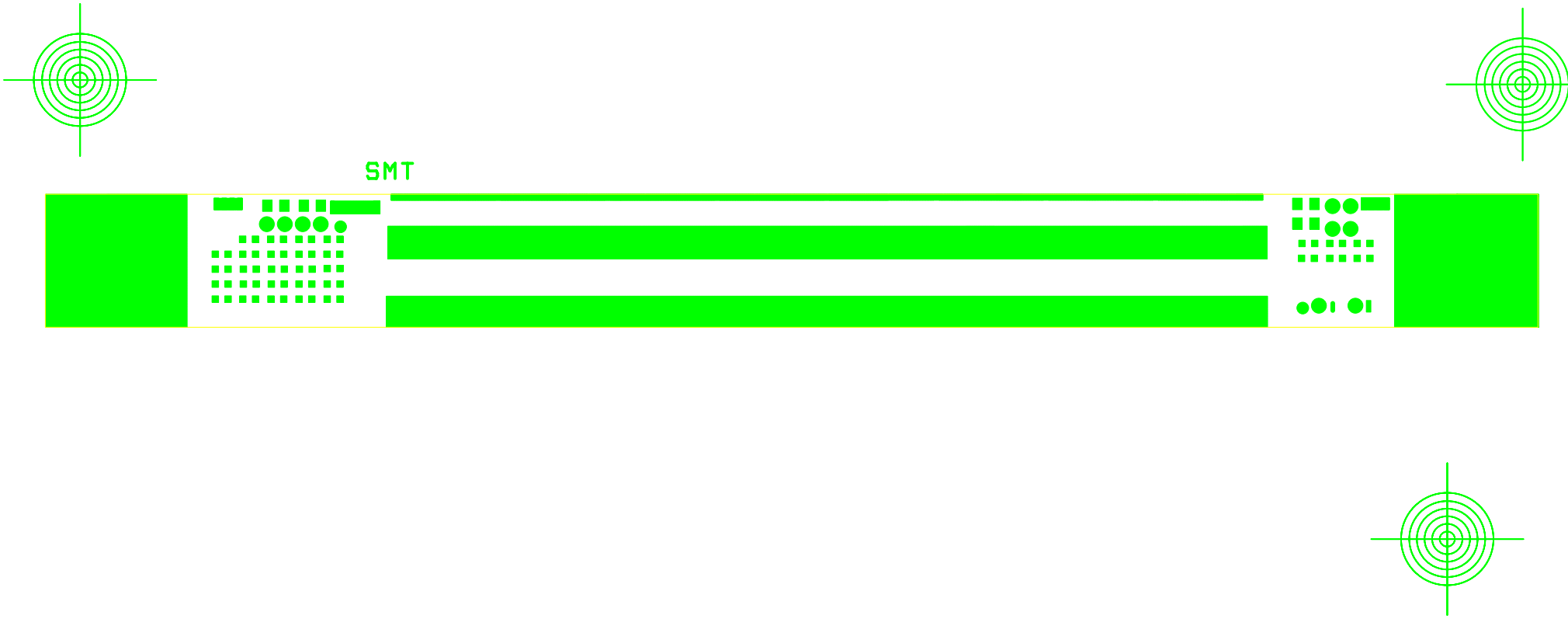
50um traces with 50um clearance (minimum)
small vias are 150um via pad with 70um hole
copper can be within 125um of Kapton edge
100 ohm differential impedance for broadside coupled traces
with trace pairs one on top of the other on IN1 & IN2
referenced to copper planes on TOP & BOT
100 ohm differential impedance for edge coupled traces on IN1
referenced to copper plane on TOP
Kapton and dielectric thickness should be adjusted for this impedance
impedance and thicknesses are to be approved by Fermilab before fabrication
adhesiveless Kapton is to be used unless Fermilab approves
Kapton flex circuit with top and bottom soldermask
pads must be plated for aluminum wedge ultrasonic wire bonding (ENIG)

this plating is normally 150 microinches of nickel
with 7 to 10 microinches of gold over the nickel

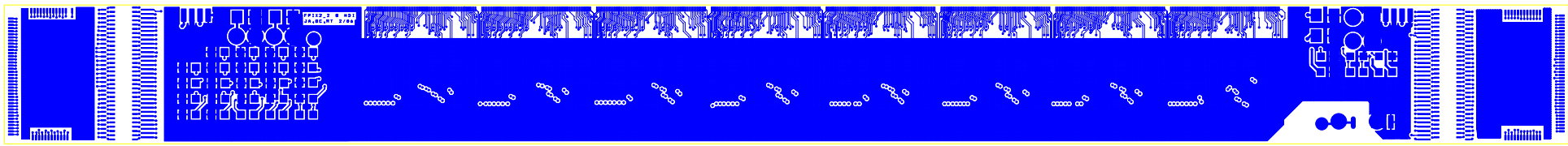
the top soldermask is critical as I.C.s connected to GND
will be shorting signals if vias are not covered
there is no soldermask in the tab areas

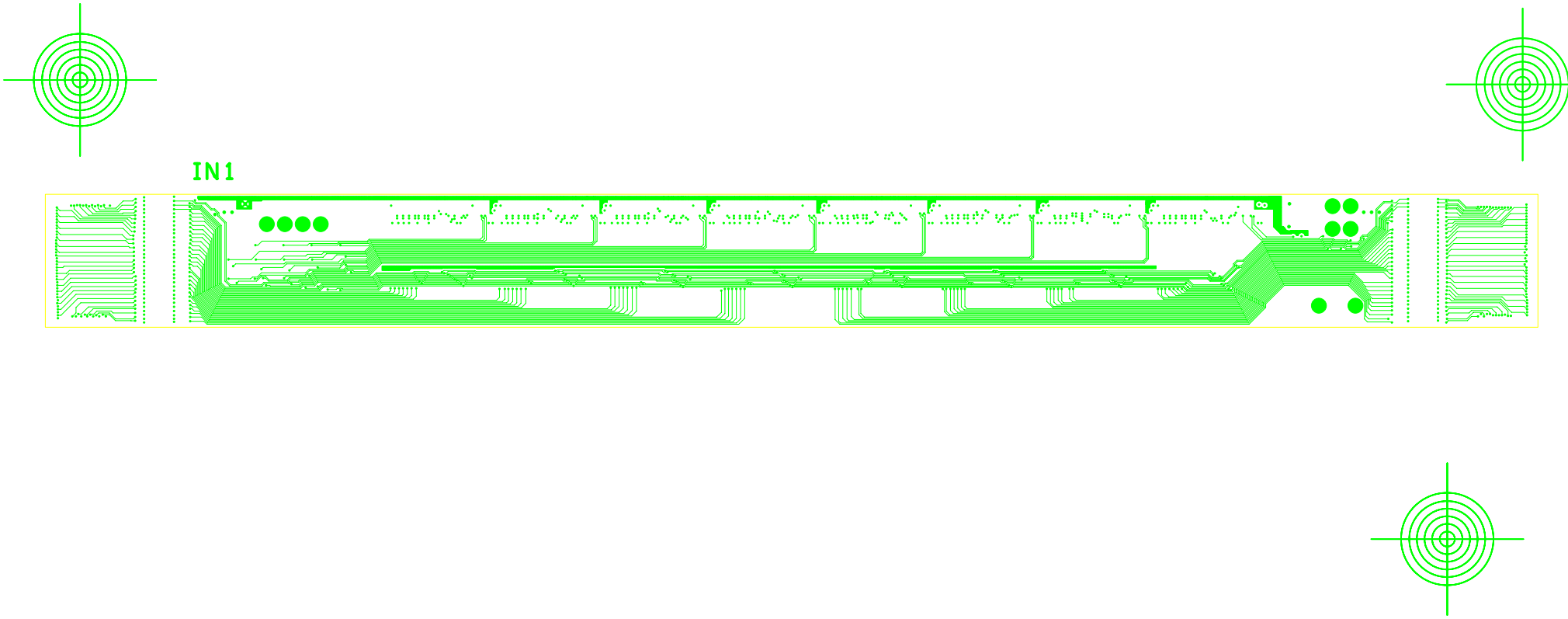
Design is to be tested for connectivity including opens and shorts
There should be no copper in tab cut off area

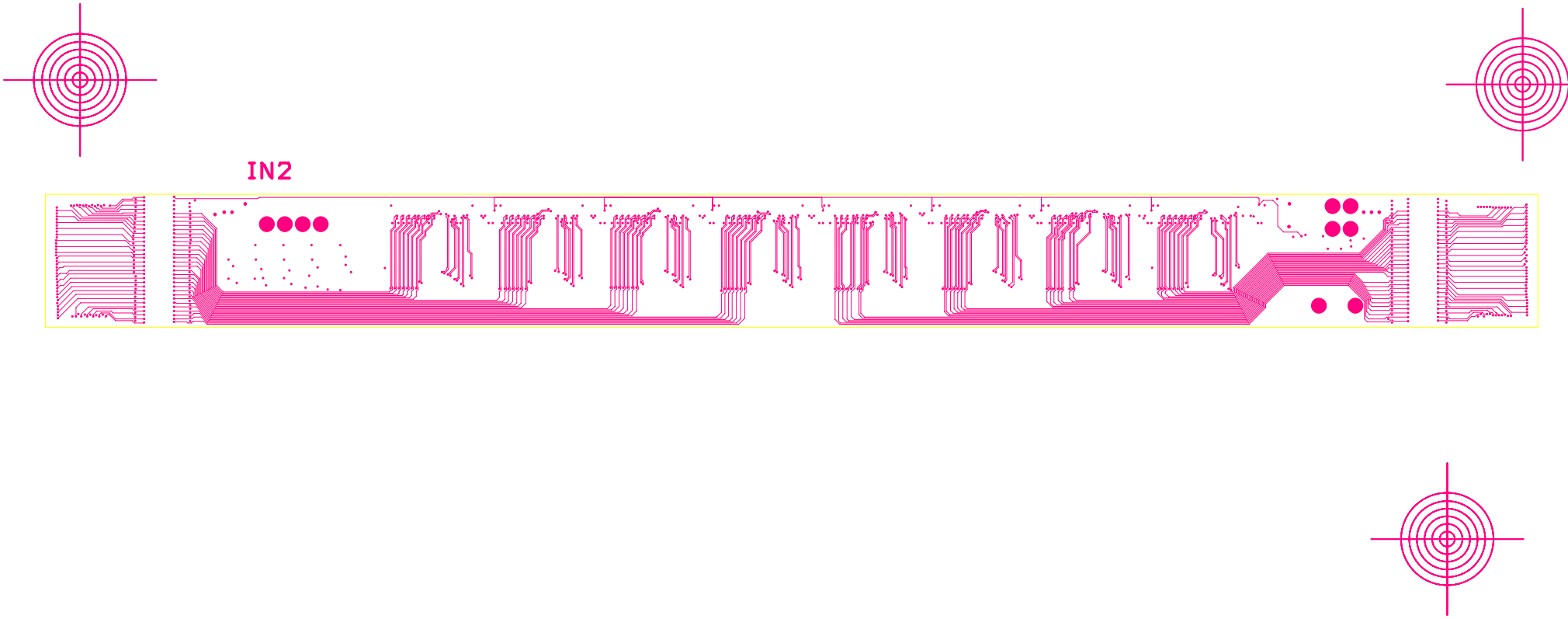

M1
M2
M3
U8
U7
U6
U5
U4
U3
U2
U1
silkscreen layer for documentation purposes only
10000
104541
10000


SMT

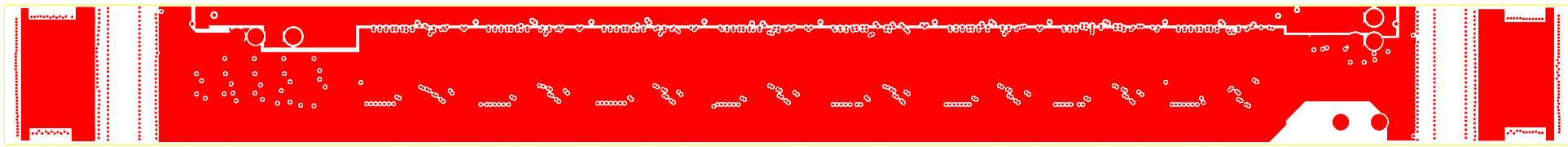
TOP

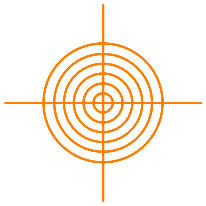
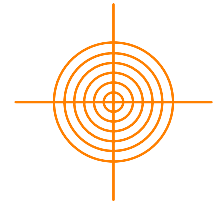



IN1


IN2

BOT





SMB